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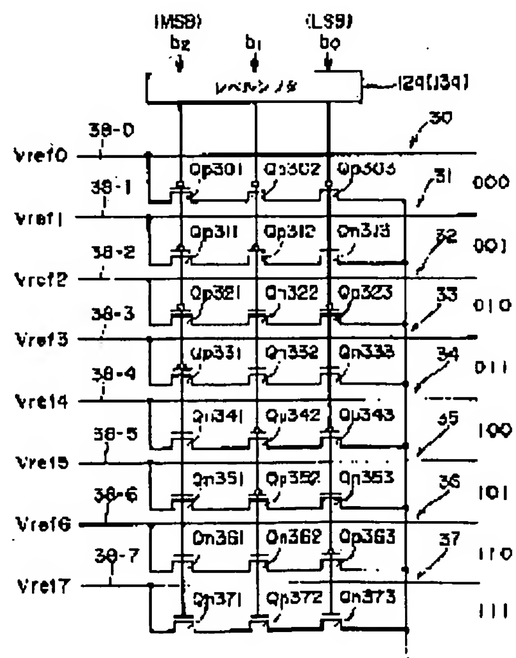
(54) DIGITAL-ANALOG CONVERTING CIRCUIT AND LIQUID CRYSTAL DISPLAY DEVICE MOUNTING THE CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a DA converting circuit which requires a small number of components composing the circuit and can contribute to narrowing the frame width of a LCD panel, and a liquid crystal display device mounting the circuit.
SOLUTION: In the reference voltage selective AD converting circuit in a liquid crystal display device integral with a driving circuit, each of three pieces of analog switches of polarities corresponding to each bit logic of, for example, three bits (b2, b1, b0) of data is formed of one piece of conductive (P-channel/N- channel) MOS transistor corresponding to each bit logic, and these are connected in series to form gradation selecting units 30-37 for as many as 8 gradations. And, these gradation selecting units 30-37 are connected across reference voltage lines 38-0 to 38-7 for as many as 8 gradations and the column line 25n, respectively.



CLAIMS

[Claim(s)]
[Claim 1]It comes to connect n polar analog switches corresponding to logic of each bit of a data signal of n bit (n is two or more integers) in series mutually, And a digital-to-analog conversion circuit having the gradation selection unit of 2^n individual connected between each of a reference voltage line of 2^n book, and an output line, respectively.
[Claim 2]The digital-to-analog conversion circuit according to claim 1, wherein said n analog switches consist of one MOS transistor of a conductivity type corresponding to logic of each bit of said data signal respectively.
[Claim 3]The digital-to-analog conversion circuit according to claim 2 which is characterized by being more than a level range where only a threshold of an N-channel metal oxide semiconductor transistor is high low [a threshold of a P channel MOS transistor] to a level range of reference voltage as for amplitude of said data signal.
[Claim 4]The 1st substrate with which a valid pixel area which consists of two or more pixels, and a drive circuit including a digital-to-analog conversion circuit were formed.
The 2nd substrate by which the placed opposite was carried out with a predetermined interval to said 1st substrate.
A liquid crystal layer held between said 1st substrate and said 2nd substrate.
Are the above the liquid crystal display which it had, and said digital-to-analog conversion circuit, It comes to connect n polar analog switches corresponding to logic of each bit of a data signal of n bit (n is two or more integers) in series mutually, And it has the gradation selection unit of 2^n individual connected, respectively between a reference voltage line of 2^n book, and a column line of a picture element part.

[Claim 5]The liquid crystal display according to claim 4 driving each pixel of said valid pixel area by common inversion driving which reverses common voltage impressed common to a counterelectrode of a liquid crystal cell for every horizontal period.
[Claim 6]Both that it is characterized by comprising the following said 1st and 2nd level shift circuit, Make a CMOS latch cell into basic constitution, have the resistance element inserted, respectively between two input parts of said CMOS latch cell, and two input signal sources, and said 1st latch circuitry, The 1st switch that made a CMOS latch cell basic constitution and was connected, respectively between two input parts of said CMOS latch cell, and two input signal lines, The 2nd switch connected between power source lines the power supply side of said CMOS latch cell, Have a control means which carries out switching control of said 1st switch and said 2nd switch complementarily, and said 2nd latch circuitry, The 1st and 2nd switch that chooses the 1st and 2nd power supply from which makes a CMOS latch cell basic constitution, it is provided at least in one side by the side of a positive supply of said CMOS latch cell, and a negative supply, and power supply voltage differs, respectively, The liquid crystal display according to claim 4 provided with a control means which carries out switching control of said 1st and 2nd switch according to each period of latch operation of said CMOS latch cell,

and output operation.
A shift register which outputs a sampling pulse sequentially from each transfer stage by said drive circuit's consisting of two or more transfer stages, answering a start signal, and performing a shift action.
The 1st latch circuitry that samples a data signal one by one and latches it from each transfer stage of said shift register synchronizing with a sampling pulse outputted.
A signal sampled by said 1st latch circuitry is latched for every horizontal period corresponding to each column line, The 1st level shift circuit that the 2nd latch circuitry that supplies the latched signal to said digital-to-analog conversion circuit is provided, and said shift register carries out the level shift of said start signal, and is supplied to a transfer stage of the first rank.
The 2nd level shift circuit that carries out the level shift of the clock signal, and is supplied to a transfer stage of each stage.

[Claim 7]Said drive circuit between said 2nd latch circuitry and said digital-to-analog conversion circuit, Provide a level shift circuit which carries out the level shift of the signal latched in said 2nd latch circuitry, and is supplied to said digital-to-analog conversion circuit, and said level shift, The liquid crystal display according to claim 6 having the resistance element which made a CMOS latch cell basic constitution and was inserted, respectively between two input parts of said CMOS latch cell, and two input signal sources.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention about the liquid crystal display (LCD;Liquid Crystal Display) which carries a digital-to-analog conversion circuit and this, The drive circuit which includes reference voltage selection type a digital-to-analog conversion circuit and this digital-to-analog conversion circuit especially as a switching element which is each pixel. Poly-Si TFT (thin film transistor; thin film transistor) is related with what is called a drive circuit integral-type liquid crystal display really formed on the substrate arranged by matrix form.
[0002]
[Description of the Prior Art]The conventional example of the drive circuit integral-type liquid crystal display which really forms a digital interface drive circuit on the same substrate as a picture element part by TFT is shown in drawing 34. As opposed to the valid pixel area 701 where matrix form comes to arrange a pixel in the figure, The 1st and 2nd level drive system 702,703 is allotted to the upper and lower sides, and the vertical-drive system 704 is allotted to the left-hand side of a figure, and it has composition really formed on the same substrate (an LCD panel is called hereafter) with the valid pixel area 701 by TFT.
[0003]The 1st level drive system 702 is constituted by the horizontal shift register 721, the sampling & 1st latch circuitry 722, the 2nd latch circuitry 723, and the DA (digital analog) conversion circuit 724. The 2nd level drive system 703 as well as the 1st level drive system 702 is constituted by the horizontal shift register 731, the sampling & 1st latch circuitry 732, the 2nd latch circuitry 733, and DA conversion circuit 734. The vertical-drive system 74 is constituted by the vertical shift register 741.
[0004]
[Problem(s) to be Solved by the Invention]When the drive circuit integral-type liquid crystal display of the above-mentioned composition is created here, the field area which really forms a drive circuit on an LCD panel, i.e., the size of the field (this is hereafter called a frame) of the periphery of the valid pixel area 701, poses a big problem. Especially the circuit area of DA conversion circuit 724,734 serves as an important point at the time of deciding the size of the frame of an LCD panel. As a DA conversion circuit of a drive circuit integral-type liquid crystal display, a reference voltage selection type is used widely. The reason is because dispersion in output potential is small.
[0005]An example of the circuitry of a reference voltage selection type DA conversion circuit is shown in drawing 35. This example of a circuit shows the case of the DA conversion circuit composition of triplet 8 gradation. This DA conversion circuit has the composition of having formed the gradation selection unit 708-0 to 708-7 which consists of the selecting switch 705, the latch circuitry 706, and the decode circuit 707 in each gradation (reference voltage Vref0-Vref7) of every so that clearly from drawing 35.
[0006]However, in the reference voltage selection type DA conversion circuit of this composition. Since the latch circuitry 706 and the decode circuit 707 are formed for every gradation and the element number which constitutes a circuit increases dramatically so that clearly from the circuitry of drawing 35, If it is really going to form the DA conversion circuit of multi-tone by TFT, when a very big circuit area is needed and it carries in a

liquid crystal display as a result, the technical problem that the frame of an LCD panel becomes large and serves as hindrance of a miniaturization of the whole device occurs.
[0007]On the other hand, in order to attain reduction of a circuit area, taking the circuitry which combined the switched capacitor with the reference voltage selection type DA conversion circuit is also considered. However, in the case of this circuitry, since a buffer circuit is needed, only a part to consume in a buffer circuit has the technical problem that increase of the power consumption of the whole system is caused.
[0008]in light of the above-mentioned problems, this invention comes out. The purpose is to provide the liquid crystal display which carries the DA conversion circuit and this which can contribute to narrow-ization of the frame of an LCD panel, without there being few element numbers to constitute, ending and moreover increasing power consumption.

[0009]
[Means for Solving the Problem]It comes to connect n polar analog switches corresponding to logic of each bit of a data signal of n bit (n is two or more integers) in a DA conversion circuit by this invention in series mutually, And it has composition of having the gradation selection unit of 2^n individual connected between each of a reference voltage line of 2^n book, and an output line, respectively. And this reference voltage selection type DA conversion circuit is carried as a DA conversion circuit which constitutes a part of that drive circuit in a drive circuit integral-type liquid crystal display.
[0010]In a liquid crystal display which carries a DA conversion circuit of the above-mentioned composition, and this, By a gradation selection unit of composition of that n polar analog switches corresponding to logic of each bit of a data signal were connected in series mutually being connected between a reference voltage line and a column line of a picture element part. Formation becomes possible with the same transistor about a decode circuit which decodes a data signal, and a selecting switch which chooses reference voltage corresponding based on the decode output. Therefore, only the part will have few element numbers which constitute a circuit, and will end.
[0011]
[Embodiment of the Invention]Hereafter, an embodiment of the invention is described in detail with reference to drawings. Drawing 1 is a block diagram showing the system configuration of the drive circuit integral-type liquid crystal display concerning one embodiment of this invention. In drawing 1, to the valid pixel area 11 where matrix form comes to arrange a pixel, the 1st and 2nd level drive system 12 and 13 is allotted to the upper and lower sides, and the vertical-drive system 14 is allotted to the left-hand side of the figure.
[0012]It is not necessary to necessarily arrange to the upper and lower sides of the valid pixel area 11 about a level drive system, and may be up-and-down arrangement of only one side. About a vertical-drive system, it may be arrangement on the right-hand side of a figure, or may be arrangement of both sides. And the 1st and 2nd level drive systems 12 and 13 and vertical-drive system 14 are really formed on the same substrate (the 1st substrate) as the valid pixel area 11 by TFT (thin film transistor). The placed opposite of the 2nd substrate (not shown) is carried out with the predetermined interval to this substrate. And the liquid crystal layer is held among both boards.
[0013]The 1st level drive system 12 is constituted by the horizontal shift register 121, the sampling & 1st latch circuitry 122, the 2nd latch circuitry 123, the level shifter 124, and DA conversion circuit (DAC) 125. The 2nd level drive system 13 as well as the 1st level drive system 12 is constituted by the horizontal shift register 131, the sampling & 1st latch circuitry 132, the 2nd latch circuitry 133, the level shifter 134, and DA conversion circuit 135. The vertical-drive system 14 is constituted by the vertical shift register 141.
[0014]An example of the composition of each pixel 20 in the valid pixel area 11 is shown in drawing 2. The pixel 20 comprises TFT21 which is a switching element, the liquid crystal cell 22 by which the picture element electrode was connected to the drain electrode of this TFT21, and the auxiliary capacity 23 with which one electrode was connected to the drain electrode of TFT21. TFT21 of each pixel 20 is connected to low (line) line

-- in which that gate electrode is a vertical selection line, column (sequence) line [in which it is connected to 24 m-1 or 24 m, 24m+1, and --, and that source electrode is a signal wire]--, 25n-1 or 25 n, 25n+1, and -- in this pixel structure.
[0015]The counterelectrode of the liquid crystal cell 22 is connected to the common line 26 with which common voltage VCOM is given. Here, what is called a common inversion driving method that reverses common voltage VCOM to every 1H (one horizontal period) is taken as a method of driving the liquid crystal cell 22, for example. Since the polarity of common voltage VCOM is reversed for everyH by using this common inversion driving method, voltage lowering of the 1st and 2nd level drive system 12 and 13 can be attained, and the power consumption of the whole device can be reduced.
[0016]Next, operation of each part of the 1st and 2nd level drive system 12 and 13 is explained. Although the following explanation takes and explains the 1st level drive system 12 to an example, the same thing can completely be said also about the 2nd level drive system 13.
[0017]In the 1st level drive system 12, horizontal transfer pulse 1, i.e., horizontal start pulse HST, 1 and horizontal clock pulse HCK1 are given to the horizontal shift register 121. Then, the horizontal shift register 121 answers horizontal start pulse HST1, and performs a horizontal scanning with the cycle of horizontal clock pulse HCK1. The sampling & 1st latch circuitry 122 latches the data which sampled digital data one by one and sampled it further synchronizing with the horizontal scanning of the horizontal shift register 121 to column line --, 25n-1 or 25 n, 25n+1, and every --.
[0018]The 2nd latch circuitry 123 answers the latch signal which can be given 1H cycle, and re-latches the latch data corresponding to the column line latched in the sampling & 1st latch circuitry 122 for everyH. About the latch data re-latched in the 2nd latch circuitry 123, the level shifter 124 carries out the level shift of the signal level (amplitude) to a predetermined level, and supplies it to DA conversion circuit 125. The level shifted in this level shifter 124 is mentioned later.
[0019]On the other hand, in the vertical-drive system 14, the vertical transfer pulse VST, i.e., a vertical start pulse, and the vertical clock pulse VCK are given to the vertical shift register 141. Then, the vertical shift register 141 is answering the vertical start pulse VST and performing a vertical scanning with the cycle of the vertical clock pulse VCK, and gives a line selection signal one by one per line to the valid pixel area 11.
[0020]The reference voltage selection type DA conversion circuit outputted to the column line which chooses the target reference voltage from the reference voltage for a gradation number, and corresponds in response to the data by which the level shift was carried out by the level shifter 124,134 as DA conversion circuit 125,135 of the 1st and 2nd level drive system 12 and 13 is used. The concrete circuitry of this reference voltage selection type DA conversion circuit 125,135 is a portion by which it is characterized [of this invention].
[0021]The basic constitution of a reference voltage selection type DA conversion circuit is shown in drawing 3. Here shall take and explain the case where it is circuitry for which the reference voltage Vref0-Vref7 of 8 (=2^3) gradation is prepared to an example to the digital data of a triplet (b2, b1, b0). In drawing 3, although the circuitry of the DA conversion circuit corresponding to a certain column line 25n is shown, the DA conversion circuit concerned is provided for every column line.
[0022]In drawing 3, the eight gradation selection units 30-37 are formed to the reference voltage Vref0-Vref7 of 8 gradation. These gradation selection units 30-37 have the composition that three polar (straight polarity/negative polarity) analog switches corresponding to the logic of each bit (b2, b1, b0) of digital data were connected in series mutually. namely[0023]The gradation selection unit 30 has the composition that it was connected between the reference voltage line 38-0 of Vref0, and the column line 25n, and the analog switch 301,302,303 of three negative polarity was mutually connected in series to data "000." The gradation selection unit 31 has the composition that it was connected between the reference voltage line 38-1 of Vref1, and the column line 25n, and the analog switch 311,312 of two negative polarity and the analog switch 313 of the straight polarity of one piece were mutually connected in series to data "001."
[0024]The gradation selection unit 32 is connected between the reference voltage line 38-2 of Vref2, and the column line 25n, It has the composition that the analog switch 321 of negative polarity, the analog switch 322 of

straight polarity, and the analog switch 323 of negative polarity were mutually connected in series to data "010." The gradation selection unit 33 has the composition that it was connected between the reference voltage line 38-3 of Vref3, and the column line 25n, and the analog switch 331 of one negative polarity and the analog switch 332,333 of the straight polarity of two pieces were mutually connected in series to data "011."

[0025]The gradation selection unit 34 has the composition that it was connected between the reference voltage line 38-4 of Vref4, and the column line 25n, and the analog switch 341 of the straight polarity of one piece and the analog switch 342,343 of two negative polarity were mutually connected in series to data "100." The gradation selection unit 35 is connected between the reference voltage line 38-5 of Vref5, and the column line 25n, It has the composition that the analog switch 351 of straight polarity, the analog switch 352 of negative polarity, and the analog switch 353 of straight polarity were mutually connected in series to data "101."

[0026]The gradation selection unit 36 has the composition that it was connected between the reference voltage line 38-6 of Vref6, and the column line 25n, and the analog switch 361,362 of the straight polarity of two pieces and the analog switch 363 of one negative polarity were mutually connected in series to data "110." The gradation selection unit 37 has the composition that it was connected between the reference voltage line 38-7 of Vref7, and the column line 25n, and the analog switch 371,372,373 of the straight polarity of three pieces was mutually connected in series to data "111."

[0027]Drawing 4 is a circuit diagram showing an example of concrete circuitry which realizes reference voltage selection type DA conversion circuit 125 of the basic constitution shown in drawing 3, gives identical codes to drawing 3 and an equivalent portion, and is shown. As three analog switches each of the gradation selection units 30-37 for 8 gradation, it has composition using the MOS transistor of the conductivity type (an N channel/P channel) corresponding to the logic of each bit (b2, b1, b0) of digital data.

[0028]in drawing 4, the gradation selection unit 30 was equivalent to data "000" -- both -- MOS of a P channel. (It is hereafter described as PMOS) It has composition which has arranged these in series and was created, using transistor Qp301, Qp302, and Qp303 as the analog switch 301,302,303. PMOS transistorQp311 corresponding to data "001" in the gradation selection unit 31, Qp312, and MOS of an N channel. (It is hereafter described as NMOS) It has composition which has arranged these in series and was created, using transistor Qn313 as the analog switch 311,312,313.

[0029]PMOS transistorQp321 corresponding to data "010", NMOS transistorQn322, and PMOS transistor Qp323 are used for the gradation selection unit 32 as the analog switch 321,322,323, It has composition which has arranged these in series and was created. The gradation selection unit 33 has composition which has arranged these in series and was created, using PMOS transistorQp331 corresponding to data "011" and NMOS transistorQn332, and Qn333 as the analog switch 331,332,333.

[0030]The gradation selection unit 34 has composition which has arranged these in series and was created, using NMOS transistorQn341 corresponding to data "100" and PMOS transistorQp342, and Qp343 as the analog switch 341,342,343. NMOS transistorQn351 corresponding to data "101", PMOS transistorQp352, and NMOS transistor Qn353 are used for the gradation selection unit 35 as the analog switch 351,352,353, It has composition which has arranged these in series and was created.

[0031]The gradation selection unit 36 has composition which has arranged these in series and was created, using NMOS transistorQn361 corresponding to data "110", Qn362, and PMOS transistor Qp363 as the analog switch 361,362,363. The gradation selection unit 37 has composition corresponding to data "111" which has arranged these in series and was both created using NMOS transistorQn371, Qn372, and Qn373 as the analog switch 371,372,373.

[0032]In reference voltage selection type DA conversion circuit 125 of the above-mentioned composition. Each of n polar analog switches corresponding to the logic of each bit of the digital data of n bit (n>=2), Create using one PMOS transistor or one NMOS transistor, and in the combination of a PMOS transistor and an NMOS transistor. Since the gradation selection unit of 2^n individual corresponding to the target gradation is constituted, the DA conversion circuit of multi-tone can be realized with a small area, and the LCD panel of a very narrow frame can be realized as a result. This is based on the following reasons.

[0033]** Since the selecting switch 705 and the decode circuit 707 which are shown in drawing 35 are formed with the same transistor, it is for there to be dramatically few element numbers which constitute a circuit, and to end. [in / conventionally / a circuit]
** Since it approaches and the continuously forming of the PMOS transistor and NMOS transistor which the well for isolation does not exist in TFT circuits, and serve as a switch can be carried out, it is for the occupation area of a circuit to be dramatically small and to end.
[0034]Reason for the above ** is further explained in full detail as compared with the structure of a single-crystal-silicon transistor. Here, the case where one NMOS transistor and one PMOS transistor are arranged and formed in series shall be taken and considered for an example.
[0035]First, considering the structure of a single-crystal-silicon transistor, as shown in drawing 5, The N^+ diffusion regions 42 and 43 are formed in the substrate face side of the P type silicon substrate 41 with a fixed interval, and an NMOS transistor is formed above the channel between the these N^+ diffusion regions 42 and 43 by the gate electrode 45 being arranged via the gate dielectric film 44. Here, the N^+ diffusion region 42 turns into a drain/source region, and the N^+ diffusion region 43 turns into sauce/drain area.
[0036]On the other hand, in order to adjoin an NMOS transistor and to form a PMOS transistor, the N well 46 for isolation by introduction of N type impurities is formed. And the P^+ diffusion regions 47 and 48 are formed in the substrate face side in this N well 46 with a fixed interval, and a PMOS transistor is formed above the channel between the these P^+ diffusion regions 47 and 48 by the gate electrode 49 being arranged via the gate dielectric film 44. Here, the P^+ diffusion region 47 turns into sauce/drain area, and the P^+ diffusion region 48 turns into a drain/source region.
[0037]And the P^+ diffusion region 47 which turns into the N^+ diffusion region 43, and the sauce/drain area of a PMOS transistor used as the sauce/drain area of an NMOS transistor in order to arrange both transistors in series, It is connected by the aluminum (aluminum) wiring 50 through the interlayer insulation film 49. Al electrode 51 is connected to the N^+ diffusion region 42 used as the drain/source region of an NMOS transistor, and Al electrode 52 is connected to the P^+ diffusion region 48 used as the drain/source region of a PMOS transistor.
[0038]Then, if the structure of polysilicon (polycrystalline silicon) and TFT of a bottom product gated mode is considered, for example, as shown in drawing 6, on the glass substrate 53, a fixed distance will be kept, the gate electrodes 54 and 55 will be formed, and the polysilicon layer 57 will be formed via the gate dielectric film 56 on it.
[0039]And on the silicon oxide 56 of the side of the gate electrodes 54 and 55, The diffusion zone 60 used as the diffusion zone 59, and the drain/source region of a PMOS transistor used as the diffusion zone 58 used as the drain/source region of an NMOS transistor, NMOS, and the sauce/drain area of the both sides of a PMOS transistor is formed. Al electrodes 62 and 63 are connected to the diffusion zones 58 and 60 through the interlayer insulation film 61, respectively.
[0040]So that clearly from contrast with the transistor structure of drawing 5, and the transistor structure of drawing 6 in the case of poly-Si TFT, Since the well (46) for isolation like [in the case of a single-crystal-silicon transistor] does not exist, an NMOS transistor and a PMOS transistor are approached, continuously forming becomes possible, and as a result, the occupation area of a circuit is dramatically small and ends.
[0041]By the way, in the liquid crystal display using common (VCOM) inversion driving, in the DA conversion circuit which chooses the reference voltage of the level range of 0V-5V. In order to secure the dynamic range of the reference voltage chosen when a MOS transistor is used as an analog switch as mentioned above, If the threshold of Vthp and an NMOS transistor is set to Vthn for the threshold of a PMOS transistor, the low side of a select data signal must be 0 or less V-Vthp, and the high-level side must be 5 or more V+Vthn.
[0042]Thus, only the threshold Vthp of a PMOS transistor is low to the level range of reference voltage in the amplitude of a select data signal, And the level range where only the threshold Vthn of an NMOS transistor is high (in the above-mentioned example.) Since it is necessary to set up more than 0 V-Vthp - 5 V+Vthn, in the system

configuration of drawing 1 in this embodiment. The level shifter (level shift circuit) 124,134 has been arranged in the preceding paragraph of DA conversion circuit 125,135, and the composition which attains the above-mentioned amplitude of a select data signal by the level shift in these level shifters 124,134 is taken.
[0043]According to this composition, the reference voltage selection type DA conversion circuit of a small area can be realized, without setting up highly the power supply voltage of the sampling & 1st latch circuitry 122,132. However, when the amplitude of a select data signal from the first is what satisfies the above-mentioned conditions, even if it does not form the level shifter 124,134, it is clear that the dynamic range of the reference voltage chosen is securable.
[0044]Here, the concrete circuitry of the level shift circuit used as the level shifter 124,134 is explained.
[0045]Drawing 7 is a circuit diagram showing the 1st example of a level shift circuit. CMOS inverter 71 with which the level shift circuit concerning this 1st example consists of NMOS transistorQn11 and PMOS transistorQp11 to which each gate and drain were connected in common, respectively, CMOS inverter 72 with which each gate and drain consist of NMOS transistorQn12 and PMOS transistorQp12 which were connected in common, respectively makes basic constitution CMOS latch cell 70 which it comes to connect in parallel mutually between the power supply VDD and a ground.
[0046]In this CMOS latch cell 70, the input edge (namely, common gate node of MOS transistorQn11 and Qp11) of CMOS inverter 71, The outgoing end (namely, drain common node of MOS transistorQn12 and Qp12) of CMOS inverter 72 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn12 and Qp12) of CMOS inverter 72 and the outgoing end (namely, drain common node of MOS transistorQn11 and Qp11) of CMOS inverter 71 are connected.
[0047]The resistance element R11 is connected between the input edge of CMOS inverter 71, and the 1st circuit input terminal 73, and the resistance element R12 is connected, respectively between the input edge of CMOS inverter 72, and the 2nd circuit input terminal 74. The resistance element R13 is connected between the input edge of CMOS inverter 71, and the power supply VDD, and the resistance element R14 is connected between the input edge of CMOS inverter 72, and the power supply VDD, respectively. The inverter 78 is connected [between the resistance element R12, and node ** and the 1st circuit output terminal 75 which are the common nodes of R14], respectively between node ** and the 2nd circuit output terminal 76 whose inverters 77 are the resistance element R11 and a common node of R12.
[0048]In the level shift circuit concerning the 1st example of the above-mentioned composition, signal in1 of about [3V] amplitude **** shall be inputted into the 1st circuit input terminal 73, and signal in2 of reversal of input signal in1 shall be inputted into the 2nd circuit input terminal 74.
[0049]In [if input signal in1 explains here using the timing of drawing 8 taking the case of circuit operation in case logic "1" (=****) and input signal in2 is logic "0" (=0V), for example] CMOS latch cell 70, Since current will flow in the course of a power supply VDD-> resistance element R14 -> node **-> NMOS transistor Qn11 -> ground since NMOS transistor Qn11 will be in an ON state, and PMOS transistor Qp12 will be in an ON state simultaneously, a power supply -- current flows in the course of the VDD-> PMOS transistor Qp12 -> node **-> resistance element R11 -> 2nd circuit input terminal 73.
[0050]At this time, a voltage drop arises in the resistance element R11 and R14, and the potential of node ** and ** rises by that voltage drop. That is, the DC shifts of the potential of node ** and ** are carried out. Here, for the node **, rather than node **, since the shift amount is large, by node ** and **, bigger amplitude difference than the amplitude difference of input signal in1 and in2 will be acquired.
[0051]The resistance element R13 and R14 make the operation which clarifies the operating point of CMOS inverters 71 and 72 more by carrying out bias of node ** and the **. And it is reversed with the inverter 77 and the potential of node ** is drawn from the 1st circuit output terminal 75 as the output signal out of the amplitude of VDD, it is reversed with the inverter 78 and the potential of node ** is drawn from the 2nd circuit output terminal 76 as the inversion signal xout of the output signal out.
[0052]Amplitude **** will be set to input signal in1 which is 3V, the level shift of in2 will be carried out to the output signal out of the amplitude of the power supply voltage VDD, and xout by the circuit operation mentioned

above, and it will be drawn. Level shift operation will be performed by the operation in which input signal in1 is completely contrary to the operation mentioned above when logic "0" and input signal in2 is logic "0."
[0053]Thus, two input parts of CMOS latch cell 70, i.e., each input edge of CMOS inverters 71 and 72 and two input signal sources, Namely, the resistance element R11 and R12 are connected between the two circuit input terminals 73 and 74 into which input signal in1 and in2 are inputted, Since sufficient voltage for making one each transistor which constitutes CMOS latch cell 70 by carrying out the DC shifts of input signal in1 and in2, and having made it give two input parts of CMOS latch cell 70 can be obtained, Even if it is a device with the large threshold Vth, for example, the circuit using TFT, the stable level shift operation is realizable at high speed.
[0054]And since it is only adding a resistance element, and it is good, while it is realizable with a small area to the basic circuit of CMOS latch cell 70, since level shift operation can be ensured even if it drops the power supply voltage VDD, low power consumption can be attained. By connecting the resistance element R13 and R14 also between two input parts of CMOS latch cell 70, and power supplies VDD, and having been made to carry out bias of node ** and the **, Since the operating point of CMOS inverters 71 and 72 can be clarified more, the more stable level shift operation is realizable.
[0055]Although it presupposed that the inversion signal of input signal in1 is considered as an input as input signal in2 in the level shift circuit concerning the 1st example, Since it is a translation which just distinguishes the logic of input signal in1, it is not necessary to be necessarily an inversion signal, and it is also possible to use the arbitrary direct current voltage of within the limits from 0V to the power supply voltage VDD as the reference voltage Vref of the distinction. The timing chart at the time of inputting the reference voltage Vref (0 <=Vref<=VDD) as input signal in2 is shown in drawing 9.
[0056]Although it has composition which derives the two output signals out of reversal by being noninverting, and xout in the example of a circuit of drawing 7, it may be the composition which derives only one of output signals. In this case, one side of the two inverters 77 and 78 becomes unnecessary.
[0057]Drawing 10 is a circuit diagram showing the modification of the level shift circuit concerning the 1st example, and attaches and shows identical codes among the figure to drawing 7 and an equivalent portion. In the level shift circuit concerning this modification, as the resistance element R11 of drawing 7, and R12, Each gate has composition using NMOS transistorQn13 connected to the power supply VDD, PMOS transistorQp13 by which each gate was connected to the ground as the resistance element R13 and R14 using Qn14, and Qp14.
[0058]Thus, when the resistance elements R11-R14 are realized with a transistor, operation of the circuit is also the same as the case of the circuit of drawing 7. It is the same as drawing 8 and drawing 9 also about the example of timing. Although the resistance element R11 and R12 are realized by NMOS and PMOS has realized the resistance element R13 and R14 in this modification, as long as it arranges a transistor so that it may become a form equivalent to these resistance elements, whichever may be sufficient as the polarity of each transistor.
[0059]Drawing 11 is a circuit diagram showing other modifications of the level shift circuit concerning the 1st example, and attaches and shows identical codes among the figure to drawing 10 and an equivalent portion. In the level shift circuit concerning this modification, it has composition which switches NMOS transistorQn13, Qn14 and PMOS transistorQp13, and Qp14 by control signal CNTL in the circuit of drawing 10. Namely, while being impressed to each gate of NMOS transistorQn13 and Qn14, control signal CNTL of active"H" inputted into the control terminal 79 from the control circuit which is not illustrated, It is reversed with the inverter 79 and is impressed by each gate of PMOS transistorQp13 and Qp14.
[0060]By thus, the thing for which the composition which switches each transistor Qn13 of CMOS latch cell 70, Qn14, Qp13, and Qp14 by control signal CNTL is taken. When this level shift circuit is activated only when a level shift is required, and there is no necessity for a level shift, the what is called latch combination type level shift circuit holding data, i.e., input signal in, 1 and 1n a logic state two can be realized.
[0061]In this example, when the resistance elements R11-R14 were realized with a transistor, presupposed that switching control of these transistors is carried out, but. Even if it is made to carry out switching control of these switches using a switch with resistance limited as the resistance elements R11-R14, the same operation effect can be obtained.

[0062]Drawing 12 is a circuit diagram showing the modification of further others of the level shift circuit concerning the 1st example, and attaches and shows identical codes among the figure to drawing 11 and an equivalent portion. In the level shift circuit concerning this modification, it has composition which added the reset circuit 81 for deciding the initial value of CMOS latch cell 70 to be a circuit of drawing 11 further. This reset circuit 81 is constituted by PMOS transistor Qp15 connected between the power supply VDD and node **, and the gate of this PMOS transistor Qp15 is connected to the reset terminal 82.
[0063]And reset-signal Reset is given to the reset terminal 82. Here, as reset-signal Reset, as shown in the timing chart of drawing 13, the signal which rises to the timing which was late for the power supply voltage VDD is used. This reset-signal Reset can be simply generated by integrating RC integrating circuit 83 with the power supply voltage VDD, as shown, for example in drawing 14.
[0064]Thus, by adding the reset circuit 81 to the circuit of drawing 11 further, and giving reset-signal Reset which rises to the timing which was late for the power supply voltage VDD to this reset circuit 81, The initial value in CMOS latch cell 70 at the time of power supply starting can be determined. By this reset action, in this example, the potential of node ** serves as "H" level by the initial state at the time of power supply starting, and the output signal out serves as the "L" level so that clearly from the timing chart of drawing 13.
[0065]Drawing 15 is a circuit diagram showing the 2nd example of a level shift circuit. CMOS inverter 85 with which the level shift circuit concerning this 2nd example consists of NMOS transistorQn21 and PMOS transistorQp21 to which each gate and drain were connected in common, CMOS inverter 86 with which each gate and drain consist of NMOS transistorQn22 and PMOS transistorQp22 which were connected in common, It has composition which made the basic circuit CMOS latch cell 84 which it comes to connect in parallel mutually between the power supply VDD and a ground.
[0066]In this CMOS latch cell 84, the input edge (namely, common gate node of MOS transistorQn21 and Qp21) of CMOS inverter 85, The outgoing end (namely, drain common node of MOS transistorQn22 and Qp22) of CMOS inverter 86 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn22 and Qp22) of CMOS inverter 86 and the outgoing end (namely, drain common node of MOS transistorQn21 and Qp21) of CMOS inverter 85 are connected.
[0067]The resistance element R21 is connected between the input edge of CMOS inverter 85, and the 1st circuit input terminal 87, and the resistance element R22 is connected, respectively between the input edge of CMOS inverter 86, and the 2nd circuit input terminal 88. The inverter 91 is connected between the input edge of CMOS inverter 86, and the 1st circuit output terminal 89, and the inverter 92 is connected, respectively between the input edge of CMOS inverter 85, and the 2nd circuit output terminal 90.
[0068]In the level shift circuit concerning the 2nd example of the above-mentioned composition, signal in1 of about [3V] amplitude **** shall be inputted into the 1st circuit input terminal 87, and signal in2 of reversal of input signal in1 shall be inputted into the 2nd circuit input terminal 88.
[0069]Since NMOS transistor Qn21 will be in an ON state in CMOS latch cell 84 if input signal in1 takes circuit operation in case logic "1" and input signal in2 is logic "0" for an example here, for example, Since current will flow in the course of a power supply VDD-> PMOS transistor Qp21 -> NMOS transistor Qn21 -> ground and PMOS transistor Qp22 will be in an ON state simultaneously, Current flows in the course of the power supply VDD-> PMOS transistor Qp22 -> resistance element R21 -> 2nd circuit input terminal 87.
[0070]At this time, a voltage drop arises in the resistance element R21, and the potential of the input edge of CMOS inverter 85 rises by that voltage drop. That is, the DC shifts of the input potentials of CMOS inverter 85 are carried out greatly. On the other hand, since there is little current which flows out of PMOS transistorQp21, the DC shifts of the input potentials of CMOS inverter 86 are hardly carried out.
[0071]By this, in each input edge of CMOS inverters 85 and 86, bigger amplitude difference than the amplitude difference of input signal in1 and in2 will be acquired. And it is reversed with the inverter 91 and the potential of the input edge of CMOS inverter 86 is drawn from the 1st circuit output terminal 89 as the output signal out of the amplitude of VDD, It is reversed with the inverter 92 and the potential of the input edge of CMOS inverter 85 is drawn from the 2nd circuit output terminal 90 as the inversion signal xout of the output signal out.

[0072]Like the case of the circuit operation of the level shift register circuit concerning the 1st example, amplitude **** will be set to input signal in1 which is 3V, the level shift of in2 will be carried out to the output signal out of the amplitude of the power supply voltage VDD, and xout by the circuit operation mentioned above, and it will be drawn. A level shift will be performed by the operation in which input signal in1 is completely contrary to the operation mentioned above when logic "0" and input signal in2 is logic "0."

[0073]Also in the case of the level shift circuit concerning the 2nd example, instead of input signal in2, It is possible to have composition which derives only the two output signals out of reversal by being noninverting and either of the xout(s) so that it is possible to use the arbitrary direct current voltage of within the limits from 0V to the power supply voltage VDD as the reference voltage Vref of the distinction.

[0074]Drawing 16 is a circuit diagram showing the modification of the level shift circuit concerning the 2nd example, and attaches and shows identical codes among the figure to drawing 15 and an equivalent portion. In the level shift circuit concerning this modification, each gate has composition using NMOS transistorQn23 and Qn24 which were connected to the power supply VDD as the resistance element R21 of drawing 15, and R22. Thus, when the resistance element R21 and R22 are realized with a transistor, operation of the circuit is also the same as the case of the circuit of drawing 15. The same modification as the modification of drawing 11 or drawing 12 is possible also about the circuit of this drawing 16.

[0075]Next, the concrete composition of the horizontal shift register 121,131 is explained. Drawing 17 is a block diagram showing an example of the composition of the horizontal shift register 121,131.

[0076]Here, since it is easy, the transfer stage shows the example of the shift register whose number is three. That is, cascade connection of three D-FF(flip-flop) 93 -1,93-2 and 93-3 is carried out. And the level shift circuit 94 is established in D (data) input side of D-FF 93-1 of the first rank, and level shift circuit 95-1,95-2 and 95-3 are provided in each CK (clock) input side of D-FF93-1,93-of each stage 2, and 93-3, respectively.

[0077]The level shift circuit 94 is for carrying out the level shift of start signal ST of an opposite phase, and the XST to the signal of the amplitude of the power supply voltage VDD mutually [about / 3V / amplitude], for example, and giving this as a D input of D-FF 93-1 of the first rank. Level shift circuit 95-1,95-2 and 95-3 are for carrying out the level shift of clock signal CK of an opposite phase, and the XCK to the signal of the amplitude of the power supply voltage VDD mutually [about / 3V / amplitude], for example, and giving this as each CK input of D-FF93-1,93-of each stage 2, and 93-3.

[0078]In the horizontal shift register 121,131 of the above-mentioned composition, the level shift circuit of composition of having been shown in drawing 11 is used as level shift circuit 94 and 95-1,95-2 and 95-3, for example. And start signal ST and XST are inputted into the level shift circuit 94 as input signal in1 and in2, and the power supply voltage VDD is inputted into it as control signal CNTL. That is, since the level shift circuit 94 always has the circuit concerned in an active state when control signal CNTL is the power supply voltage VDD, it will function only as a level shifter.

[0079]On the other hand, to level shift circuit 95-1,95-2 and 95-3. Clock signal CK and XCK are inputted as input signal in1 and in2, and each output of OR gate 96-1,96-2 which considers the shift pulse (Q output) of the self-stage and the shift pulse (D input of the self-stage) of the preceding paragraph as two inputs, and 96-3 is inputted as control signal CNTL. Level shift circuit 95-1,95-2 and 95-3, [namely,] Only when D-FF93-1,93-of self-stage 2 and 93-3 perform a shift action, That is, only when required for transmission, a level shift is performed for clock signal CK of low-voltage amplitude, and XCK, and when other, it will function as a latch combination type latches clock signal CK and XCK and it is made not to make transmit.

[0080]Thus, by using the level shift circuit of composition of having been shown in drawing 11 as level shift circuit 94 and 95-1,95-2 and 95-3 in the horizontal shift register 121,131, Since the level shift circuit concerned can realize level shift operation stable to start signal ST of low-voltage amplitude, XST, or clock signal CK and XCK at high speed, Even if it is a case where the threshold Vth constitutes D-FF93-1,93-2 and 93-3 using a large device, for example, TFT, stable fast transmission operation can be realized.

[0081]Although it presupposed that the level shift circuit of composition of having been shown in drawing 11 is used as level shift circuit 94 and 95-1,95-2 and 95-3 in this example, It is also possible to use the level shift

circuit of composition of to have been shown in not the thing restricted to this but drawing 7, drawing 10, drawing 12, drawing 15, or drawing 16, and the same operation effect as the above-mentioned case can be obtained.
[0082]As mentioned above, in a drive circuit integral-type liquid crystal display The shift register of the above-mentioned composition as the horizontal shift register 121,131 of the level drive systems 12 and 13, Namely, by being able to realize with a small area and using the shift register of low power consumption, Drive circuits containing the horizontal shift register 121,131, such as the level drive systems 12 and 13 and the vertical-drive system 14, When creating on the same substrate as the valid pixel area 11, while being able to narrow the adjacent spaces (frame) of the valid pixel area 11 which allots the drive circuit concerned, the drive circuit integral-type liquid crystal display of low power consumption is realizable.
[0083]And in the case of the shift register of the above-mentioned composition, even if it is a device with the large threshold Vth, for example, the circuit using TFT, so that clearly from having carried out point **, there is also an advantage that the stable fast transmission operation is realizable.
[0084]Next, the concrete composition of the sampling latch circuit used as the sampling & 1st latch circuitry 122,132 of the 1st and 2nd level drive system 12 and 13 is explained.
[0085]Drawing 18 is a circuit diagram showing the 1st example of a sampling latch circuit. The sampling latch circuit concerning this 1st example, CMOS inverter 101 with which each gate and drain consist of NMOS transistorQn31 and PMOS transistorQp31 which were connected in common, respectively, CMOS inverter 102 with which each gate and drain consist of NMOS transistorQn32 and PMOS transistorQp32 which were connected in common, respectively, CMOS latch cell 100 of the comparator composition which it comes to connect in parallel mutually between the power source line 107 of the power supply voltage VDD and a ground is made into basic constitution.
[0086]In this CMOS latch cell 100, the input edge (namely, common gate node of MOS transistorQn31 and Qp31) of CMOS inverter 101, The outgoing end (namely, drain common node of MOS transistorQn32 and Qp32) of CMOS inverter 102 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn32 and Qp32) of CMOS inverter 102 and the outgoing end (namely, drain common node of MOS transistorQn31 and Qp31) of CMOS inverter 101 are connected.
[0087]The switch 105 is connected between the input edge of CMOS inverter 101, and the 1st circuit input terminal 103, and the switch 106 is connected, respectively between the input edge of CMOS inverter 102, and the 2nd circuit input terminal 104. The switch 108 is connected also between the power supply sides 107 of CMOS latch cell 100, i.e., the node A and a power source line.
[0088]Switching control of the switch 105,106 is directly done by sampling pulse SP inputted from the sampling terminal 109, and switching control of the switch 108 is carried out by the reversal pulse of sampling pulse SP who passed through the inverter 110. The inverter 114 is connected [between node ** and the 1st circuit output terminal 111 which are the input edges of CMOS inverter 102], respectively between node ** and the 2nd circuit output terminal 112 whose inverter 113 is an input edge of CMOS inverter 101.
[0089]In the sampling latch circuit concerning the 1st example of the above-mentioned composition, signal in1 of about [3V] amplitude **** is inputted into the 1st circuit input terminal 103, The arbitrary direct current voltage (reference voltage Vref) in the voltage range below or more [0] V**** shall be inputted into the 2nd circuit input terminal 104 as signal in2.
[0090]If sampling pulse SP of active"H" is inputted from the sampling terminal 109 for explaining circuit operation using the timing chart of drawing 19, here, The switch 105,106 will be in an one (close) state, and, thereby, input signal in1 and in2 will be transmitted to node [of CMOS latch cell 100] **, and **. At this time, simultaneously, since the switch 108 will be in an OFF (open) state by sampling pulse SP's reversal pulse, the power supply side (node A) of CMOS latch cell 100 is separated from the power source line 107.
[0091]Next, if sampling pulse SP disappears, node [of CMOS latch cell 100] ** and ** will be divided with the 1st and 2nd circuit input terminal 103,104, and the power supply side of CMOS latch cell 100 will be simultaneously connected to the power source line 107. Comparison processing according to the voltage of this instantaneous node ** and ** is performed by CMOS latch cell 100, and latch operation starts. Eventually, node

** will be latched to the power supply voltage VDD or 0V according to the polarity of input signal in1 of the moment sampling pulse SP disappeared. At this time, the voltage of that reverse polarity is latched to node **.
[0092]The data of input signal in1 whose amplitude **** is about 3V is sampled by the above circuit operation synchronizing with sampling pulse SP, and is latched to node ** as data of the amplitude of the power supply voltage VDD. And it is reversed with the inverter 113 and the latch data of node ** is drawn from the 1st circuit output terminal 111 as the output signal out, it is reversed with the inverter 114 and the latch data of node ** is drawn from the 2nd circuit output terminal 112 as the inversion signal xout of the output signal out.
[0093]As mentioned above, make CMOS latch cell 100 of comparator composition into basic constitution, and Two input parts (node **, **) of this CMOS latch cell 100, While connecting the switch 105,106, respectively between two input signal sources (the 1st and 2nd circuit input terminal 103,104), By connecting the switch 108 also between the power source lines 107 the power supply side (node A) of CMOS latch cell 100, and carrying out switching control of the switch 105,106 and the switch 108 complementarily, Since the direct current which current does not flow into CMOS latch cell 100 at the sampling period of input signal in1 by the switch 105,106 and in2, therefore flows at the time of operation is very few, the power consumption in this sampling latch circuit can be reduced.
[0094]At the moment of the sampling period having expired and the power supply voltage VDD being supplied to CMOS latch cell 100 through the switch 108, Since the data of input signal in1 whose amplitude **** is about 3V will be latched as data of the amplitude of the power supply voltage VDD, even if it is a case of the circuit constituted using the device with the big threshold Vth like TFT, the stable sampling & latch operation is realizable. And since it can constitute only from adding switch 105,106,108 grade to the basic circuit of CMOS latch cell 100, the sampling latch circuit which has a level shift function with a small area with a very small element number is realizable.
[0095]As input signal in2 although [in the sampling latch circuit concerning this example] the direct current voltage (reference voltage) Vref of the range of 0 <=Vref<=**** is inputted, It is not necessary to be necessarily direct current voltage, and since it is a translation which just distinguishes the logic of input signal in1, as shown in the timing chart of drawing 20, it is also possible to use the inversion signal of input signal in1 as a reference signal of the distinction. In this case, there is an advantage which can take the large margin of logic distinction of input signal in1 rather than the case where direct current voltage of the range of 0 <=Vref<=**** is made into reference voltage.
[0096]Although it has composition which derives the two output signals out of reversal by being noninverting, and xout in the example of a circuit of drawing 18, it may be the composition which derives only one of output signals. In this case, one side of the two inverters 113,114 becomes unnecessary.
[0097]Drawing 21 is a circuit diagram showing the modification of the level shift circuit concerning the 1st example, and attaches and shows identical codes among the figure to drawing 18 and an equivalent portion. In the level shift circuit concerning this modification, while using NMOS transistorQn33 and Qn34 as the switch 105,106 by the side of the signal input of drawing 18, It has the composition of impressing sampling pulse SP directly to each gate of these transistors, using PMOS transistor Qp33 as the switch 108 by the side of a power supply.
[0098]Thus, when the switch 105,106,108 is realized with a transistor, operation of the circuit is also the same as the case of the circuit of drawing 18. It is the same as drawing 19 and drawing 20 also about the example of timing. Although the switch 105,106 is realized by NMOS and PMOS has realized the switch 108 in this modification, when sampling pulse SP is active"L", the polarity of become [reverse] is clear.
[0099]Drawing 22 is a circuit diagram showing the 2nd example of a sampling latch circuit. The sampling latch circuit concerning this 2nd example, CMOS inverter 151 with which each gate and drain consist of NMOS transistorQn41 and PMOS transistorQp41 which were connected in common, respectively, CMOS inverter 152 with which each gate and drain consist of NMOS transistorQn42 and PMOS transistorQp42 which were connected in common, respectively, CMOS latch cell 150 of the comparator composition which it comes to connect in parallel mutually between the power source line 157 and a ground is made into basic constitution.
[0100]In this CMOS latch cell 150, the input edge (namely, common gate node of MOS transistorQn41 and Qp41)

of CMOS inverter 151, The outgoing end (namely, drain common node of MOS transistorQn42 and Qp42) of CMOS inverter 152 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn42 and Qp42) of CMOS inverter 152 and the outgoing end (namely, drain common node of MOS transistorQn41 and Qp41) of CMOS inverter 151 are connected.
[0101]The switch 155 is connected between the input edge of CMOS inverter 151, and the 1st circuit input terminal 153, and the switch 156 is connected, respectively between the input edge of CMOS inverter 152, and the 2nd circuit input terminal 154. The switch 158 is connected also between the power supply sides 157 of CMOS latch cell 150, i.e., the node A and a power source line. Switching control of the switch 155,156 is directly done by sampling pulse SP inputted from the sampling terminal 159, and switching control of the switch 158 is carried out by the reversal pulse of sampling pulse SP who passed through the inverter 160.
[0102]The inverter 164 is connected [between node ** and the 1st circuit output terminal 161 which are the input edges of CMOS inverter 152], respectively between node ** and the 2nd circuit output terminal 162 whose inverter 163 is an input edge of CMOS inverter 151. The inverter 163 has CMOS inverter composition which consists of P, NMOS transistorQp43, and Qn43 which each gate and a drain were connected in common, respectively, and were connected between the node A and the ground. The inverter 154 also has CMOS inverter composition which consists of P, NMOS transistorQp44, and Qn44 which each gate and a drain were connected in common, respectively, and were similarly connected between the node A and the ground.
[0103]In the sampling latch circuit concerning the 2nd example of the above-mentioned composition, signal in1 of about [3V] amplitude **** shall be inputted into the 1st circuit input terminal 153, and the arbitrary direct current voltage within the limits below or more [0] V**** shall be inputted into the 2nd circuit input terminal 154 as signal in2. About the circuit operation of the sampling latch circuit concerning this 2nd example, it is fundamentally [as it of the sampling latch circuit concerning the 1st example] the same.
[0104]That is, if sampling pulse SP of active"H" is inputted from the sampling terminal 159, the switch 155,156 will be in an one (close) state, and, thereby, input signal in1 and in2 will be transmitted to node [of CMOS latch cell 150] **, and **. At this time, simultaneously, since the switch 158 will be in an OFF (open) state by sampling pulse SP's reversal pulse, the power supply side of CMOS latch cell 150 is separated from the power source line 157.
[0105]Next, if sampling pulse SP disappears, node [of CMOS latch cell 150] ** and ** will be divided with the 1st and 2nd circuit input terminal 153,154, and the power supply side of CMOS latch cell 150 will be simultaneously connected to the power source line 157. Comparison processing according to the voltage of this instantaneous node ** and ** is performed by CMOS latch cell 150, and latch operation starts. Eventually, node ** will be latched to the power supply voltage VDD or 0V according to the polarity of input signal in1 of the moment sampling pulse SP disappeared. At this time, the voltage of that reverse polarity is latched to node **.
[0106]The data of input signal in1 whose amplitude **** is about 3V is sampled by the above circuit operation synchronizing with sampling pulse SP, and is latched to node ** as data of the amplitude of the power supply voltage VDD. And it is reversed with the inverter 163 and the latch data of node ** is drawn from the 1st circuit output terminal 161 as the output signal out, it is reversed with the inverter 164 and the latch data of node ** is drawn from the 2nd circuit output terminal 162 as the inversion signal xout of the output signal out.
[0107]According to the composition of the sampling latch circuit concerning this 2nd example, it adds to the operation effect by the sampling latch circuit concerning the 1st example that carried out point **, Since the unnecessary current which flows into CMOS inverter 163,164 by carrying out switching control like [current supply / to CMOS inverter 163,164] CMOS latch cell 150 is reducible, the power consumption in this sampling latch circuit can be reduced further.
[0108]Also in the case of the sampling latch circuit concerning the 2nd example, like [in the case of the modification of the 1st example shown in drawing 21], It is also possible to have composition which derives only the two output signals out of the reversal of the switch 155,156,158 realizable with a transistor by it being noninverting in using the inversion signal of input signal in1 as input signal in2 and either of the xout(s).
[0109]The sampling latch circuit which starts the 1st and 2nd example of the above-mentioned composition in a

drive circuit integral-type liquid crystal display as the sampling & 1st latch circuitry 122,132 of the 1st and 2nd level drive system 12 and 13 as mentioned above, Namely, by being able to realize with a small area and using the sampling latch circuit of low power consumption, Drive circuits, such as the 1st and 2nd level drive system 12 and 13 including the sampling latch circuit concerned and the vertical-drive system 14, When creating on the same substrate as the valid pixel area 11, while being able to narrow the frame of the valid pixel area 11 which allots the drive circuit concerned, the drive circuit integral-type liquid crystal display of low power consumption is realizable.
[0110]And in the case of the sampling latch circuit of the above-mentioned composition, even if it is a device with the large threshold Vth, for example, the circuit using TFT, so that clearly from having carried out point **, there is also an advantage that the stable sampling & latch operation is realizable.
[0111]Drawing 23 is a block diagram showing an example of the concrete composition of the sampling & 1st latch circuitry constituted using the sampling latch circuit of the above-mentioned composition, for example, shows the case where the digital data b0 of a triplet, b1, and b2 are considered as an input. Here, although the sampling & 1st latch circuitry 122 by the side of the 1st level drive system 12 is shown, the composition is completely the same also about the sampling & 1st latch circuitry 132 by the side of the 2nd level drive system 13.
[0112]Sampling latch circuit 122-1,122-2,122-3 is formed every bit of the digital data b0, b1, and b2 so that clearly from drawing 23. Each bit data of the digital data b0, b1, and b2 are inputted into these sampling latch circuit 122-1,122-2,122-3 as input signal in1, and the reference voltage (direct current voltage) Vref is inputted into it common to each circuit as input signal in2. And according to sampling pulse SP outputted from the horizontal shift register 121, the sampling of the data signal b0 of low-voltage amplitude, b1, and b2 is performed.
[0113]The level shift of the signal sampled in each of this sampling latch circuit 122-1,122-2,122-3 is carried out to the signal of high-tension amplitude required for TFT circuits, and it is latched to it. And the signal of this latched high-tension amplitude, Line sequential operation is carried out by 2nd latch circuitry 123-1,123-2,123-3 of the next step provided for every bit of digital data like sampling latch circuit 122-1,122-2,122-3, After passing through the level shift 124 (refer to drawing 1) which is not illustrated, it is outputted to the column line with which the valid pixel area 11 corresponds through DA converter 125.
[0114]Here, it is required that sampling latch circuit 122-1,122-2,122-3 can be dramatically dedicated into a small area. The horizontal length assigned to one sampling latch unit serves as a dot pitch/number of bits in the composition of the drive circuit integral-type liquid crystal display shown in drawing 1, and is very short. Therefore, the sampling latch circuit which starts each above-mentioned example realizable with a small area as sampling latch circuit 122-1,122-2,122-3 which can satisfy this condition will become very effective.
[0115]Although it has the composition of inputting the reference voltage (direct current voltage) Vref common to each circuit as input signal in2, in the example of a circuit of drawing 23, As it explained also in the sampling latch circuit concerning the 1st example, and shown in drawing 24, it is also possible to input the data signal b0, b1, inversion signal xb0 of b2, xb1, and xb2 every sampling latch circuit 122-1,122-2,122-3.
[0116]Drawing 25 is a block diagram showing the modification of drawing 24, and attaches and shows identical codes among the figure to drawing 24 and an equivalent portion. In this modification, the switch (equivalent to the switch 108 of drawing 18 and the switch 158 of drawing 22) by the side of the power supply of each sampling latch circuit 122-1,122-2,122-3 is shared between each circuit 122-1,122-2,122-3, It has the composition of having realized this switch for example, by PMOS transistor Qp45.
[0117]Since according to the above-mentioned composition two switches by the side of a power supply can be reduced when digital data is a triplet, the further small area-ization of a circuit is attained. It is good like the case of the example of a circuit of drawing 23 also considering the reference voltage Vref of direct current voltage as input signal in2 [common to each sampling latch circuit 122-1,122-2,122-3] to replace with inversion signal xb0, xb1, and xb2.
[0118]Next, the concrete composition of the latch circuitry used as the 2nd latch circuitry 123,133 of the 1st and 2nd level drive system 12 and 13 is explained.
[0119]Drawing 26 is a circuit diagram showing the 1st example of latch circuitry. CMOS inverter 171 with which the latch circuitry concerning this 1st example consists of N-channel metal oxide semiconductor transistor Qn51

and P channel MOS transistor Qp51 to which each gate and drain were connected in common, respectively, CMOS inverter 172 with which each gate and drain consist of NMOS transistorQn52 and PMOS transistorQp52 which were connected in common, respectively makes basic constitution CMOS latch cell 170 which it comes to connect in parallel mutually.

[0120]In this CMOS latch cell 170, the input edge (namely, common gate node of MOS transistorQn51 and Qp51) of CMOS inverter 171, The outgoing end (namely, drain common node of MOS transistorQn52 and Qp52) of CMOS inverter 172 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn52 and Qp52) of CMOS inverter 172 and the outgoing end (namely, drain common node of MOS transistorQn51 and Qp51) of CMOS inverter 171 are connected.

[0121]The switch 175 is connected between the input edge of CMOS inverter 171, and the 1st circuit input terminal 173, and the switch 176 is connected between the input edge of CMOS inverter 172, and the 2nd circuit input terminal 174. The outgoing end of CMOS inverter 172 is connected to the 1st circuit output terminal 177, and the outgoing end of CMOS inverter 171 is connected to the 2nd circuit output terminal 178, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminal 177,178.

[0122]As for the positive supply side of this CMOS latch cell 170, direct continuation of the node A is carried out to the power source line 179 of the positive power supply voltage VDD. While being connected to the power source line 182 of negative supply side voltage (for example, grand level) VSS1 via the switch 180, a negative supply side the node B, It is connected to the power source line 183 of power-supply-voltage (negative supply voltage) VSS2 lower than power-supply-voltage VSS1 via the switch 181.

[0123]Switching control of the switch 180 is carried out with the switch 175,176 by output enable pulse oe1 inputted into the input terminal 184 from the control circuit which is not illustrated. On the other hand, switching control of the switch 181 is carried out by output enable pulse oe2 inputted into the input terminal 185 from the above-mentioned control circuit.

[0124]In the latch circuitry concerning the 1st example of the above-mentioned composition, signal in1 with the amplitude of VDD-VSS1 shall be inputted into the 1st circuit input terminal 173, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 174. Here, the circuit operation of the latch circuitry concerning the 1st example is explained using the timing chart of drawing 27.

[0125]First, if output enable pulse oe1 of active"H" is inputted into the input terminal 174, this will be answered, the switch 175,176 will be in an one (close) state, input signal in1 and in2 will be sampled, and it will transmit to CMOS latch cell 170. Thereby, input signal in1 and in2 are once latched to CMOS latch cell 170 with the amplitude of VDD-VSS1.

[0126]While the switch 180 answers output enable pulse oe1 and is in an ON state in the period of this latch operation, Since output enable pulse oe2 is in the reverse polarity ("L" level) of output enable pulse oe1 and the switch 181 is in an OFF (open) state, the negative supply side of CMOS latch cell 170 will be connected to the power source line 172 of power-supply-voltage VSS1.

[0127]Next, while output enable pulse oe1 changes on the "L" level, when output enable pulse oe2 changes on "H" level, it shifts to the period of output operation. In this period, since the switch 180 will be in an OFF state and the switch 181 will be in an ON state, the negative supply side of CMOS latch cell 170 will be connected to the power source line 183 of power-supply-voltage VSS2.

[0128]By this, in CMOS latch cell 170, the signal latched with the amplitude of VDD-VSS1 till then will have the amplitude of VDD-VSS2. And the signal of the amplitude of this VDD-VSS2 will be outputted as signal out1 and out2. As a result, the sampling latch of signal in1 with the amplitude of VDD-VSS1 and in2 can be carried out, and level conversion (level shift) can be carried out to signal out1 with the amplitude of VDD-VSS2, and out2.

[0129]As mentioned above, in the latch circuitry concerning a 1st embodiment. In the latch circuitry which makes CMOS latch cell 170 basic constitution, and has a level shift function, The two switches 180,181 which choose VSS1 power supply and VSS2 power supply as the negative supply side of CMOS latch cell 170 are formed, By carrying out switching control of these switches 180,181 according to each period of the latch operation of CMOS

latch cell 170, and output operation, by the period of latch operation, CMOS latch cell 170 will operate with VSS1 power supply, and will operate with VSS2 power supply in the period of output operation.
[0130]In order for many of charging current for being able to control by this the current which flows into the power supply of VSS1/VSS2, and charging especially output load to flow toward VSS1 power supply from a VDD power supply, there is dramatically little current which flows into VSS2 power supply. And while latch operation and level shift operation are realizable with the small number of circuit elements, Since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends, the latch circuitry with a level shift function of small-area-izing is realizable.
[0131]Another example of timing is shown in drawing 28. In the example of timing of drawing 28, falling of output enable pulse oe2 a little rather than the standup of output enable pulse oe1 Early, The standup of output enable pulse oe2 is late a little rather than falling of output enable pulse oe1. By using such timing relationship, the current which flows into VSS2 power supply can be reduced certainly.
[0132]Drawing 29 is a circuit diagram showing the example of the latch circuitry concerning the 1st example, and attaches and shows identical codes among the figure to drawing 26 and an equivalent portion. In the latch circuitry concerning this example, as the switch 175,176,180,181 of drawing 26, NMOS transistorQn53, Qn54, Qn55, and Qn56 are used, It has the composition of impressing output enable pulse oe1 to each gate of transistor Qn53, Qn54, and Qn55, and impressing output enable pulse oe2 to the gate of transistor Qn56, respectively.
[0133]Thus, when the switch 175,176,180,181 is realized with a transistor, operation of the circuit is also the same as the case of the circuit of drawing 26. It is the same as drawing 27 and drawing 28 also about the example of timing. Although NMOS has realized the switch 175,176,180,181 in this example, when output enable pulse oe1 and oe2 are active"L", it is clear the polarity's to become reverse.
[0134]Drawing 30 is a circuit diagram showing the 2nd example of latch circuitry. CMOS inverter 191 with which the latch circuitry concerning this 2nd example consists of NMOS transistorQn61 and PMOS transistorQp61 to which each gate and drain were connected in common, respectively, CMOS inverter 192 with which each gate and drain consist of NMOS transistorQn62 and PMOS transistorQp62 which were connected in common, respectively makes basic constitution CMOS latch cell 190 which it comes to connect in parallel mutually.
[0135]In this CMOS latch cell 190, the input edge (namely, common gate node of MOS transistorQn61 and Qp61) of CMOS inverter 191, The outgoing end (namely, drain common node of MOS transistorQn62 and Qp62) of CMOS inverter 192 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn62 and Qp62) of CMOS inverter 192 and the outgoing end (namely, drain common node of MOS transistorQn61 and Qp61) of CMOS inverter 191 are connected.
[0136]The switch 195 is connected between the input edge of CMOS inverter 191, and the 1st circuit input terminal 193, and the switch 196 is connected between the input edge of CMOS inverter 192, and the 2nd circuit input terminal 194. The outgoing end of CMOS inverter 192 is connected to the 1st circuit output terminal 197, and the outgoing end of CMOS inverter 191 is connected to the 2nd circuit output terminal 198, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminal 197,198.
[0137]As for the positive supply side of this CMOS latch cell 190, the node A is connected to the power source line 202 of power-supply-voltage VDD2 higher than power-supply-voltage VDD1 via the switch 200 while being connected to the power source line 201 of positive-supply-voltage VDD1 via the switch 199. As for the negative supply side, direct continuation of the node B is carried out to the power source line 203 of negative supply side voltage (for example, grand level) VSS.
[0138]Switching control of the switch 199 is carried out with the switch 195,196 by output enable pulse oe1 inputted into the input terminal 204 from the control circuit which is not illustrated. On the other hand, switching control of the switch 200 is carried out by output enable pulse oe2 inputted into the input terminal 205 from the above-mentioned control circuit.
[0139]In the latch circuitry concerning the 2nd example of the above-mentioned composition, signal in1 with the

amplitude of VDD1-VSS shall be inputted into the 1st circuit input terminal 193, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 194. The pulse in the timing relationship of drawing 27 or drawing 28 as well as as output enable pulse oe1 and oe2 the case of the latch circuitry concerning the 1st example is inputted.
[0140]Thereby, in the latch circuitry concerning the 2nd example, the fundamentally same operation as the latch circuitry concerning the 1st example is performed. That is, in the period of latch operation with active output enable pulse oe1, it operates under VDD1 power supply and signal in1 with the amplitude of VDD1-VSS and in2 are once latched with the same amplitude as CMOS latch cell 190 through the switch 195,196.
[0141]Next, output enable pulse oe2 in the period of active output operation. Since the power supply by the side of right [of CMOS latch cell 190] switches from VDD1 power supply to VDD2 power supply, the level shift of the signal with the amplitude of VDD1-VSS will be carried out to the signal of the amplitude of VDD2-VSS, and this will be drawn as output signal out1 and out2.
[0142]As mentioned above, in the latch circuitry concerning the 2nd example. The two switches 199,200 for power supply selection are formed in the positive supply side of CMOS latch cell 190, By carrying out switching control of these switches 199,200 according to each period of the latch operation of CMOS latch cell 190, and output operation, In order to operate with VDD1 power supply in the period of latch operation and to operate with VDD2 power supply in the period of output operation, While being able to control the current which flows into the power supply of VDD1/VDD2 as well as the case of the 1st example and being able to constitute from a small number of circuit elements moreover, Since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends, small area-ization is attained.
[0143]Drawing 31 is a circuit diagram showing the 3rd example of latch circuitry. CMOS inverter 211 with which the latch circuitry concerning this 3rd example consists of NMOS transistorQn71 and PMOS transistorQp71 to which each gate and drain were connected in common, respectively, CMOS inverter 212 with which each gate and drain consist of NMOS transistorQn72 and PMOS transistorQp72 which were connected in common, respectively makes basic constitution CMOS latch cell 210 which it comes to connect in parallel mutually.
[0144]In this CMOS latch cell 210, the input edge (namely, common gate node of MOS transistorQn71 and Qp71) of CMOS inverter 211, The outgoing end (namely, drain common node of MOS transistorQn72 and Qp72) of CMOS inverter 212 is connected, Furthermore, the input edge (namely, common gate node of MOS transistorQn72 and Qp72) of CMOS inverter 212 and the outgoing end (namely, drain common node of MOS transistorQn71 and Qp71) of CMOS inverter 211 are connected.
[0145]The switch 215 is connected between the input edge of CMOS inverter 211, and the 1st circuit input terminal 213, and the switch 216 is connected between the input edge of CMOS inverter 212, and the 2nd circuit input terminal 214. The outgoing end of CMOS inverter 212 is connected to the 1st circuit output terminal 217, and the outgoing end of CMOS inverter 211 is connected to the 2nd circuit output terminal 218, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminal 217,218.
[0146]As for the positive supply side of this CMOS latch cell 210, the node A is connected to the power source line 222 of power-supply-voltage VDD2 higher than power-supply-voltage VDD1 via the switch 220 while being connected to the power source line 221 of positive-supply-voltage VDD1 via the switch 219. While being connected to the power source line 225 of negative supply side voltage (for example, grand level) VSS1 via the switch 223, a negative supply side the node B, It is connected to the power source line 226 of power-supply-voltage (negative supply voltage) VSS2 lower than power-supply-voltage VSS1 via the switch 224.
[0147]Switching control of the switch 219,223 is carried out with the switch 215,216 by output enable pulse oe1 inputted into the input terminal 227 from the control circuit which is not illustrated. On the other hand, switching control of the switch 220,224 is carried out by output enable pulse oe2 inputted into the input terminal 228 from the above-mentioned control circuit.
[0148]In the latch circuitry concerning the 3rd example of the above-mentioned composition, signal in1 with the

amplitude of VDD1-VSS shall be inputted into the 1st circuit input terminal 213, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 214. The pulse in the timing relationship of drawing 27 or drawing 28 as well as as output enable pulse oe1 and oe2 the case of the latch circuitry concerning the 1st and 2nd example is inputted.

[0149]Thereby, in the latch circuitry concerning the 3rd example, the fundamentally same operation as the latch circuitry concerning the 1st and 2nd example is performed. Namely, output enable pulse oe1 in the period of active latch operation. It operates under each power supply of VDD1 and VSS1, and signal in1 with the amplitude of VDD1-VSS1 and in2 are once latched with the same amplitude as CMOS latch cell 210 through the switch 215,216.

[0150]Next, output enable pulse oe2 in the period of active output operation. While the power supply by the side of right [of CMOS latch cell 210] switches from VDD1 power supply to VDD2 power supply, Since the power supply of a negative side switches from VSS1 power supply to VSS2 power supply, the level shift of the signal with the amplitude of VDD1-VSS1 will be carried out to the signal of the amplitude of VDD2-VSS2, and this will be drawn as output signal out1 and out2.

[0151]As mentioned above, in the latch circuitry concerning the 3rd example. The two switches 219,220 and the switch 223,224 are formed in the positive supply [of CMOS latch cell 210], and negative supply side as an object for power supply selection, respectively, By carrying out switching control of these switches 219,220 and the switch 223,224 according to each period of the latch operation of CMOS latch cell 210, and output operation, In the period of latch operation, it operates with each power supply of VDD1 and VSS1, and in the period of output operation, since it will operate with each power supply of VDD2 and VSS2, the current which flows into each power supply as well as the case of the 1st and 2nd example can be controlled. And since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends while being able to constitute from a small number of circuit elements, small area-ization is attained.

[0152]About the latch circuitry concerning the 2nd and 3rd example of the above as well as the example (refer to drawing 29) of the 1st example. The switch 195,196,199,200 in drawing 30 and the switches 215, 216, and 219,220,223,224 in drawing 31 are realizable with a transistor. However, each inversion signal of output enable pulse oe1 and oe2 will be used as a signal with which a PMOS transistor is preferred and switches these in this case as the switch 199,200 in drawing 30, and the switch 219,220 in drawing 31.

[0153]Although it had composition which derives two output signal out1 which is an inversion signal mutually, and out2 in the latch circuitry concerning the 1st, 2nd, and 3rd example, it may be the composition which derives only one of output signals.

[0154]As mentioned above, in a drive circuit integral-type liquid crystal display The 1st, the latch circuitry with a level shift function of the above-mentioned composition as the 2nd latch circuitry 123,133 of the 2nd level drive system 12 and 13, Namely, by being able to realize with a small area and using the latch circuitry of low power consumption, When creating drive circuits including the latch circuitry concerned, such as the level drive systems 12 and 13 and the vertical-drive system 14, on the same substrate as the valid pixel area 11, while being able to narrow the frame of the valid pixel area 11 which allots the drive circuit concerned, the drive circuit integral-type liquid crystal display of low power consumption is realizable.

[0155]Drawing 32 is a block diagram showing an example of the concrete composition at the time of using the latch circuitry (refer to drawing 26) which starts the 1st example among each example mentioned above as the 2nd latch circuitry 123,133, for example, shows the example in the case of inputting the digital data b0 of a triplet, b1, and b2. Here, although the 2nd latch circuitry 123 by the side of the 1st level drive system 12 is shown, the composition is completely the same also about the 2nd latch circuitry 133 by the side of the 2nd level drive system 13.

[0156]Sampling latch circuit 122-1,122-2,122-3 is formed every bit of the digital data b0, b1, and b2, and latch circuitry 123-1,123-2,123-3 is further formed in the latter part, respectively so that clearly from drawing 32. Sampling latch circuit 122-1,122-2,122-3, Each bit data of the digital data b0, b1, and b2 are considered as an

input, and each input data is sampled according to the sampling pulse outputted from the horizontal shift register 121 (refer to drawing 1).

[0157]On the other hand, to latch circuitry 123-1,123-2,123-3. While each sampling data are supplied from sampling latch circuit 122-1,122-2,122-3, Output enable pulse oe1 outputted from the buffer 230 based on the latch pulse inputted from the outside and oe2 are inputted as a latch pulse, and it has the composition that VSS2 power supply is further supplied as the 2nd power supply of a negative side from the 2nd power generation circuit 231.

[0158]By this latch circuitry 123-1,123-2,123-3, After answering output enable pulse oe1 and carrying out the sampling latch of each sampling data of sampling latch circuit 122-1,122-2,122-3 of the preceding paragraph, Level conversion to signal amplitude required for the synchronization (formation of line sequential) of data and the DA translation of the next step is performed in the timing of output enable pulse oe2, After carrying out a level shift by the level shifter 124 (refer to drawing 1) which is not illustrated, it outputs to the column line with which the valid pixel area 11 corresponds through DA converter 125.

[0159]Thus, by using the latch circuitry concerning each above-mentioned example as the 2nd latch circuitry 123,133 in a drive circuit integral-type liquid crystal display, In the latch circuitry concerned, since he is trying to use a power supply properly in each period of latch operation/output operation, the current which flows into the 2nd power generation circuit 231 can be controlled. Since the 2nd latch circuitry 123,133 is realizable with a small area by this while built-in(one formation)-ization to the liquid crystal panel of the 2nd power generation circuit 231 becomes easy, narrow picture frame-ization of a liquid crystal panel is attained.

[0160]drawing 33 is a block diagram showing the modification of drawing 32, and attaches and shows identical codes among the figure to drawing 32 and an equivalent portion -- it is. In this modification, the switch 232,233 is formed as a switch (equivalent to the switch 180,181 of drawing 26) by the side of the negative supply of each latch circuitry 123-1,123-2,123-3, It has composition which shared this switch 232,233 between each circuit 123-1,123-2,123-3.

[0161]According to this composition, digital data in the example of a triplet. As opposed to the switch for two pieces and a total of six power supply changes in the switch by the side of a negative supply being required to each of three latch circuitry corresponding to a triplet, when the circuit of drawing 26 is used as it was, Since it will end with two switches to three latch circuitry and four switches for a power supply change can be reduced, the further small area-ization is attained and, therefore, narrow picture frame-ization can be realized from that of a liquid crystal panel.

[0162]Although it presupposed that the latch circuitry concerning the 1st example is used as the 2nd latch circuitry 123,133 in this example, it is also possible to use the latch circuitry concerning the 2nd and 3rd example, and the same operation effect can be obtained.

[0163]As mentioned above, although the concrete example of the horizontal shift register 121,131, the sampling & latch circuitry 122,132, the 2nd latch circuitry 123,133, the level shifter 124,134, and DA conversion circuit 125,135 was described, Each circuit of a liquid crystal display does not need to adopt the circuitry concerning these each example simultaneously, it is also possible to have composition which adopted the circuitry which requires one of circuits for each above-mentioned example, and in this case, even if it is, it can contribute to narrow picture frame-ization of an LCD panel.

[0164]

[Effect of the Invention]In the drive circuit integral-type liquid crystal display which carries a reference voltage selection type DA conversion circuit and this according to this invention as explained above, n polar analog switches corresponding to the logic of each bit of the data signal of n bit the gradation selection unit of 2^n individual which it comes to connect in series mutually, By having connected, respectively between each of the reference voltage line of 2^n book, and the column line of a picture element part, Since there are few element numbers which formation of is attained with the same transistor in the decode circuit which decodes a data signal, and the selecting switch which chooses reference voltage corresponding based on the decode output, and

constitute a circuit and they end, The LCD panel of a very narrow frame can be realized without increasing power consumption.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the system configuration of the drive circuit integral-type liquid crystal display concerning one embodiment of this invention.
[Drawing 2]It is a circuit diagram showing an example of the composition of a valid pixel area.
[Drawing 3]It is a basic constitution figure of a reference voltage selection type DA conversion circuit.
[Drawing 4]It is a circuit diagram showing the concrete circuitry of a reference voltage selection type DA conversion circuit.
[Drawing 5]It is a sectional view showing an example of the structure of a single-crystal-silicon transistor.
[Drawing 6]It is a sectional view showing an example of the structure of poly-Si TFT.
[Drawing 7]It is a circuit diagram showing the 1st example of a level shift circuit.
[Drawing 8]It is a timing chart for explaining the circuit operation of the level shift circuit concerning the 1st example.
[Drawing 9]It is a timing chart at the time of making direct current voltage into reference voltage.
[Drawing 10]It is a circuit diagram showing the modification of the level shift circuit concerning the 1st example.
[Drawing 11]It is a circuit diagram showing other modifications of the level shift circuit concerning the 1st example.
[Drawing 12]It is a circuit diagram showing the modification of further others of the level shift circuit concerning the 1st example.
[Drawing 13]It is a timing chart for explaining the circuit operation at the time of adding a reset circuit.
[Drawing 14]It is a circuit diagram showing the example of a circuit which generates a reset signal.
[Drawing 15]It is a circuit diagram showing the 2nd example of a level shift circuit.
[Drawing 16]It is a circuit diagram showing the modification of the level shift circuit concerning the 2nd example.
[Drawing 17]It is a block diagram showing an example of the composition of a horizontal shift register.
[Drawing 18]It is a circuit diagram showing the 1st example of a sample hold circuit.
[Drawing 19]It is a timing chart for explaining the circuit operation of the sample hold circuit concerning the 1st example.
[Drawing 20]It is a timing chart at the time of setting the inversion signal of input signal in1 to input signal in2.
[Drawing 21]It is a circuit diagram showing the modification of the sample hold circuit concerning a 1st embodiment.
[Drawing 22]It is a circuit diagram showing the 2nd example of a sample hold circuit.
[Drawing 23]It is a block diagram showing an example of the concrete composition at the time of using the sample hold circuit concerning each example as the sampling & 1st latch circuitry.
[Drawing 24]It is a block diagram showing the composition at the time of setting the inversion data of digital data to input signal in2.
[Drawing 25]It is a block diagram showing the modification of drawing 24.
[Drawing 26]It is a circuit diagram showing the 1st example of latch circuitry.

[Drawing 27]It is a timing chart for explaining the circuit operation of the latch circuitry concerning a 1st embodiment.
[Drawing 28]It is a timing chart which shows another example of timing of the circuit operation of the latch circuitry concerning a 1st embodiment.
[Drawing 29]It is a circuit diagram showing the example of the latch circuitry concerning a 1st embodiment.
[Drawing 30]It is a circuit diagram showing the 2nd example of latch circuitry.
[Drawing 31]It is a circuit diagram showing the 3rd example of latch circuitry.
[Drawing 32]It is a block diagram showing an example of the concrete composition at the time of using the latch circuitry concerning each embodiment as the 2nd latch circuitry.
[Drawing 33]It is a block diagram showing the modification of drawing 32.
[Drawing 34]It is a block diagram showing the system configuration of a conventional example.
[Drawing 35]It is a circuit diagram showing an example of a reference voltage selection type DA conversion circuit.

[Description of Notations]
11 -- A valid pixel area, 12, 13 -- The 1 and 2nd level drive system, 14 -- Vertical-drive system, 20 -- A pixel, 21 -- TFT (thin film transistor), 22 -- Liquid crystal cell, 23 -- Auxiliary capacity, 30-37 -- A gradation selection unit, 70, 84,100,150,170,190 -- CMOS latch cell, 71,72,85, 86, 101,102,151, 152, 171,172,191,192 -- CMOS inverter, 121,131 -- A horizontal shift register, 122,132 -- The sampling & 1st latch circuitry (sampling latch circuit), 123,133 -- The 2nd latch circuitry (latch circuitry), 124,134 -- Level shifter (level shift circuit), 125,135 -- A DA conversion circuit, 301-303,311-313,321-323,331-333,341-343,351-353,361-363,371-373 -- An analog switch, Vref0-Vref7 -- Reference voltage

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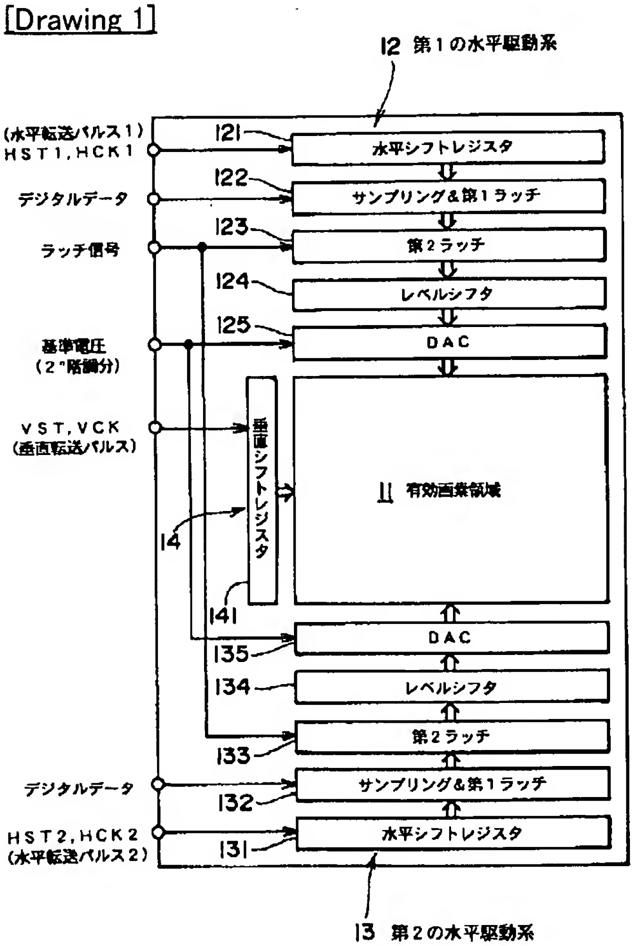
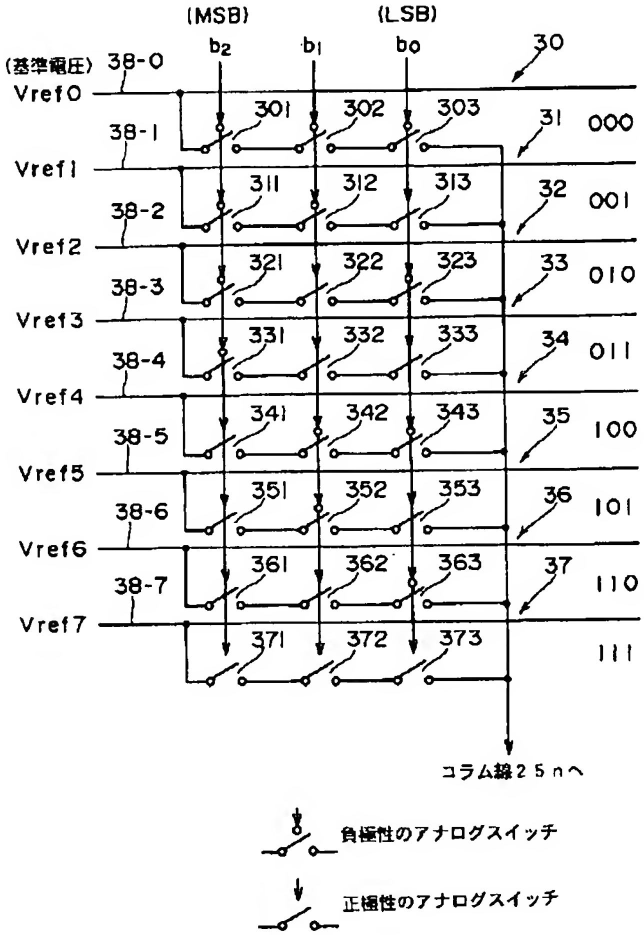
[Translation done.]

DRAWINGS

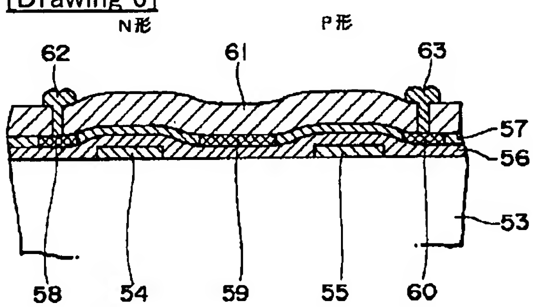
[Drawing 1]



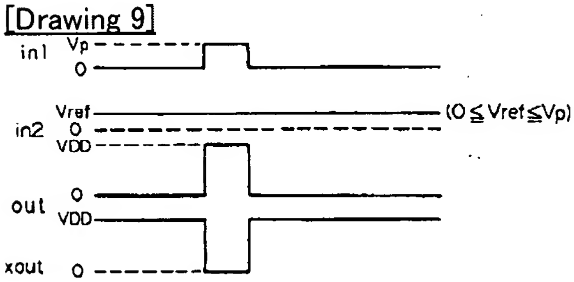
[Drawing 3]



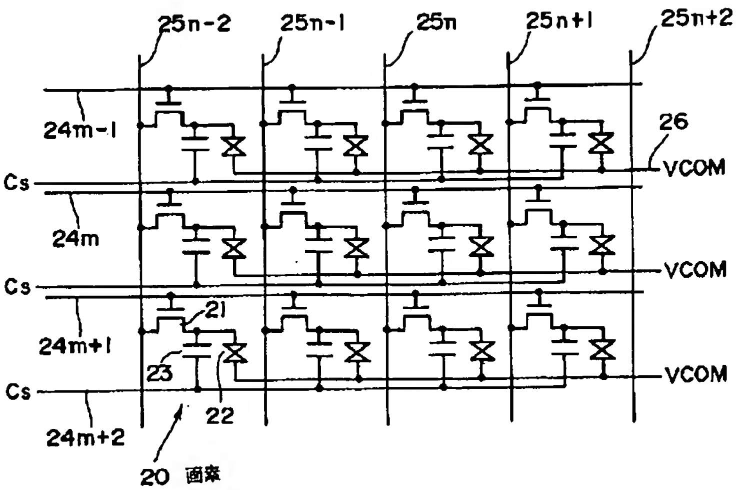
[Drawing 6]



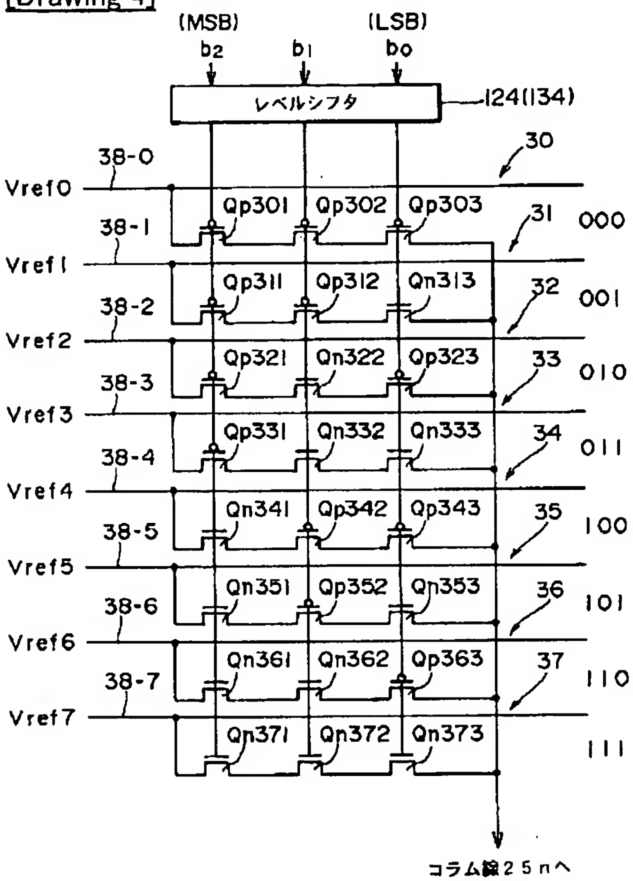
[Drawing 9]



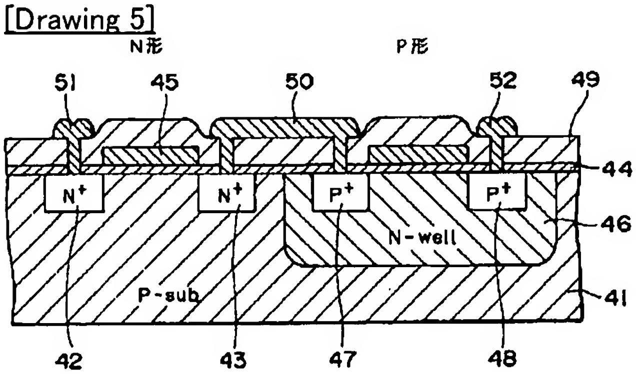
[Drawing 2]



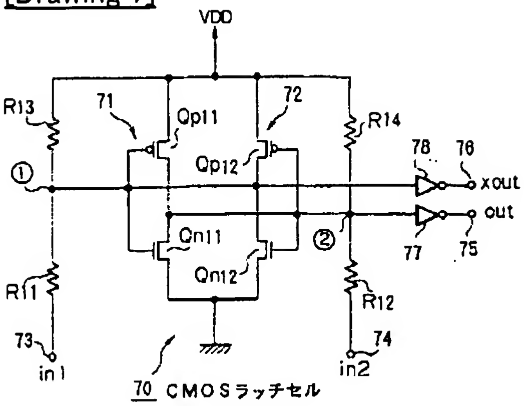
[Drawing 4]



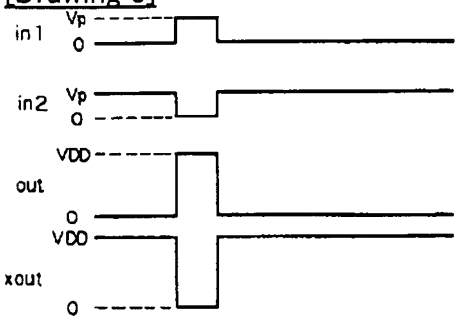
[Drawing 5]



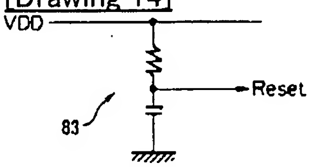
[Drawing 7]



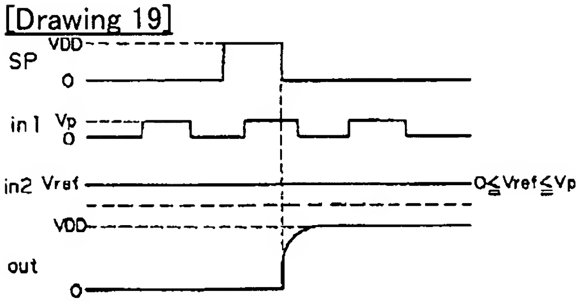
[Drawing 8]



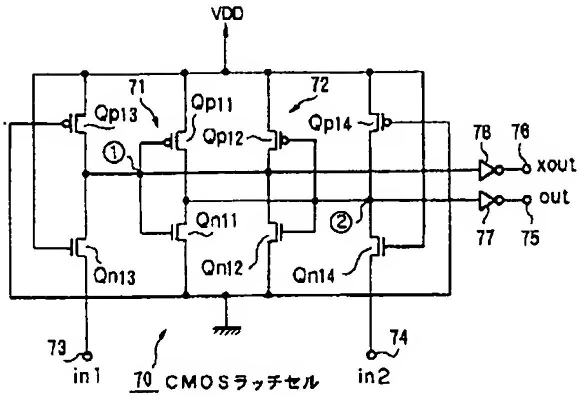
[Drawing 14]



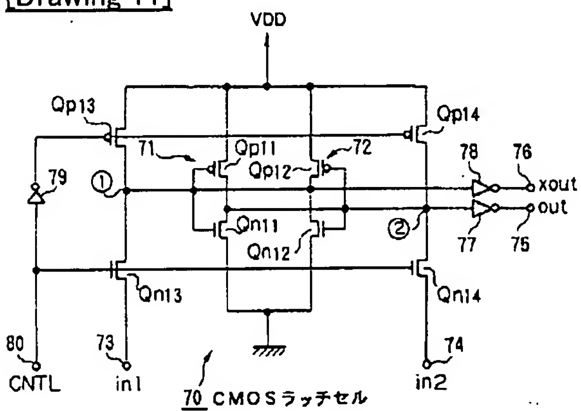
[Drawing 19]



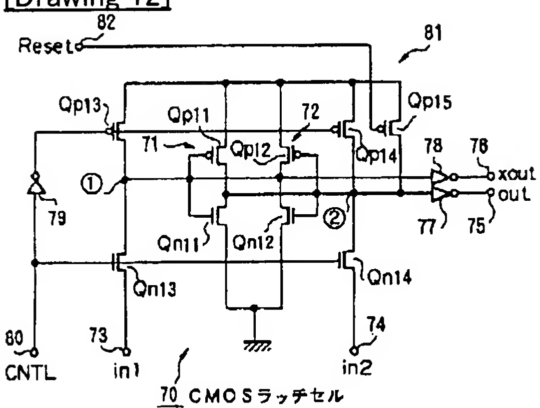
[Drawing 10]



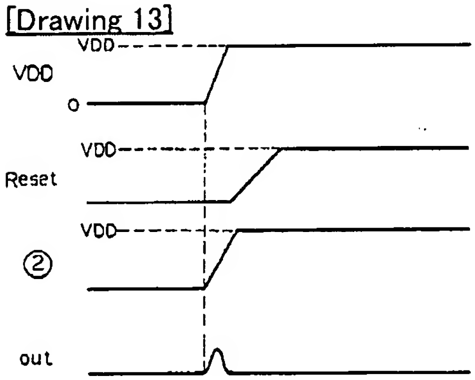
[Drawing 11]



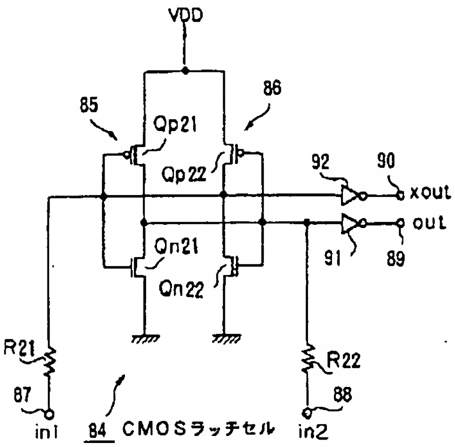
[Drawing 12]



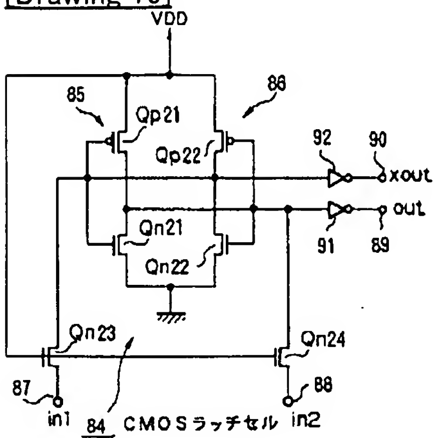
[Drawing 13]



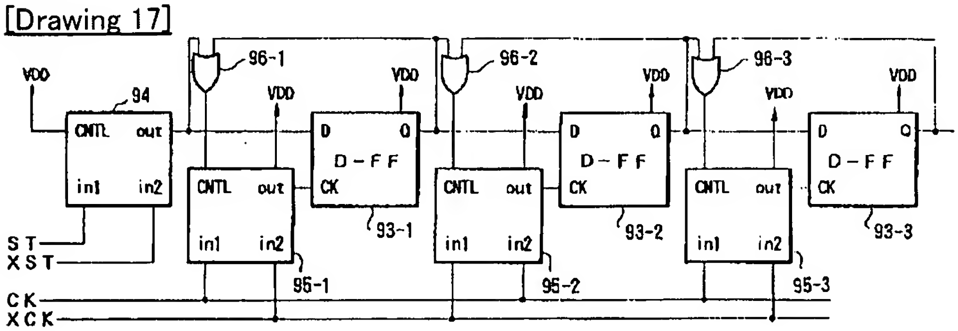
[Drawing 15]



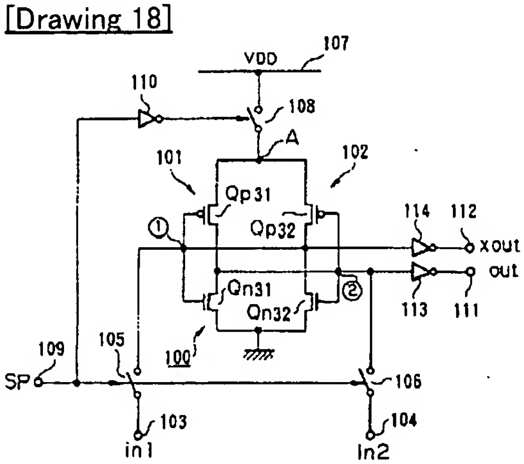
[Drawing 16]



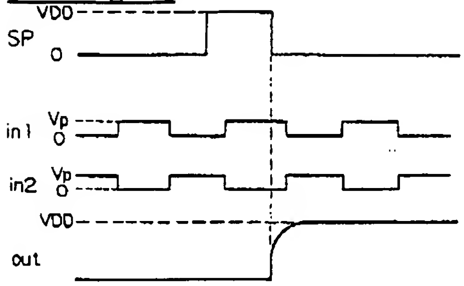
[Drawing 17]



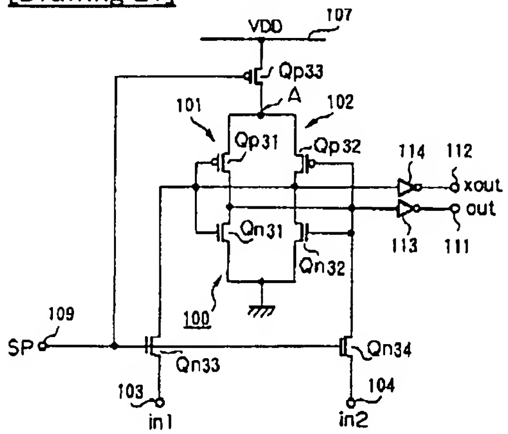
[Drawing 18]



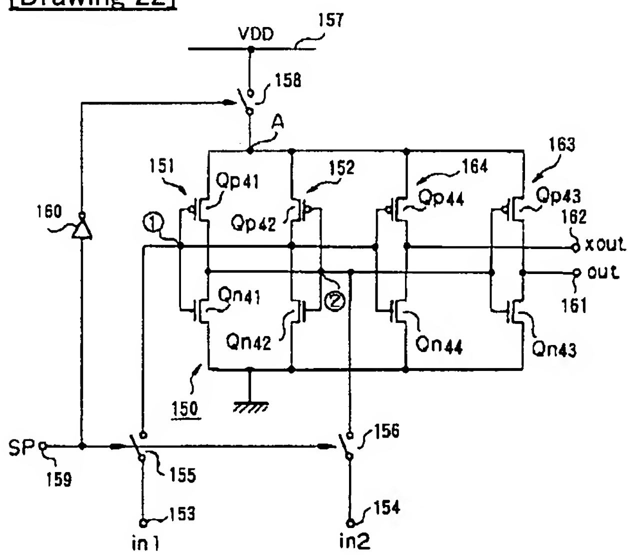
[Drawing 20]



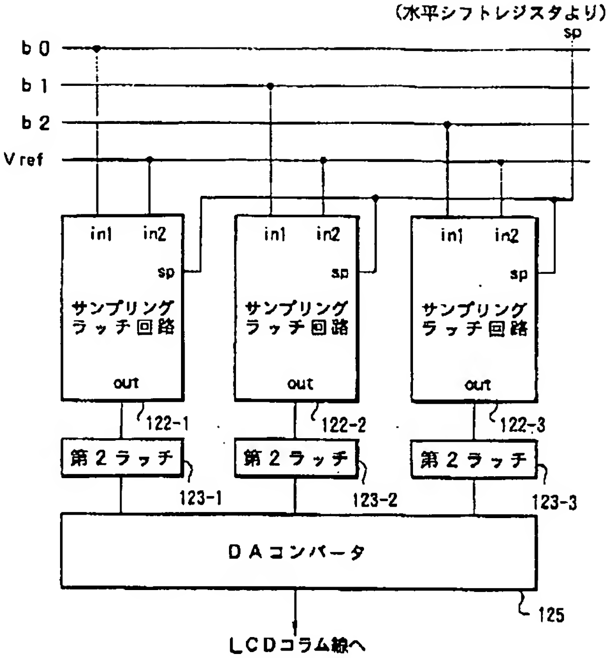
[Drawing 21]



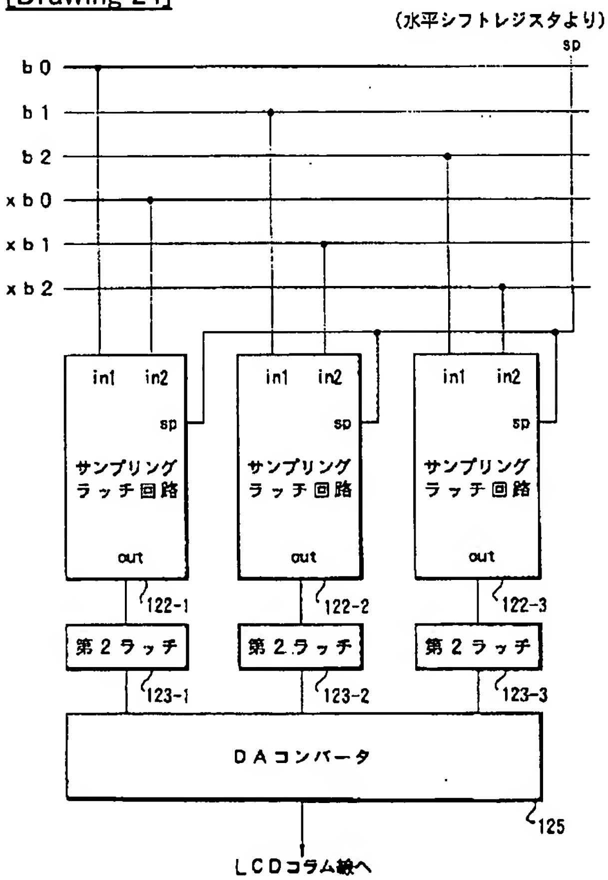
[Drawing 22]



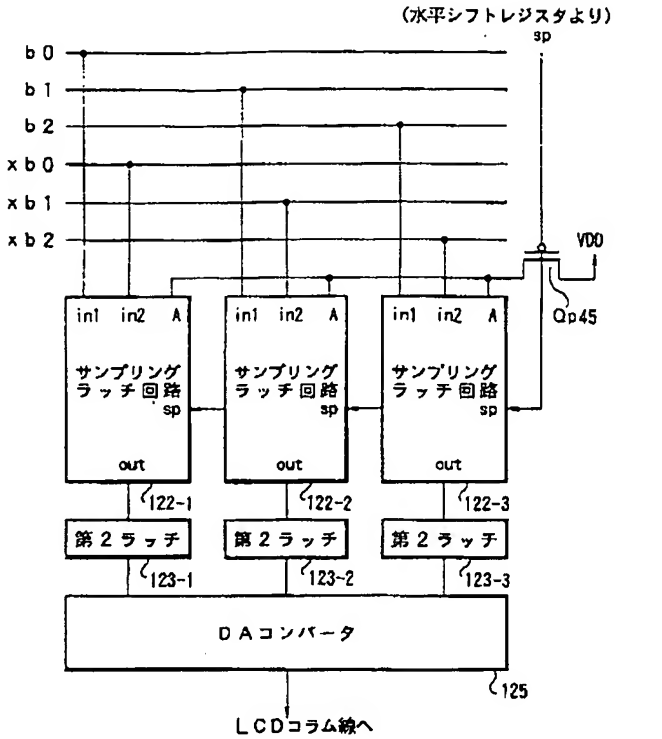
[Drawing 23]



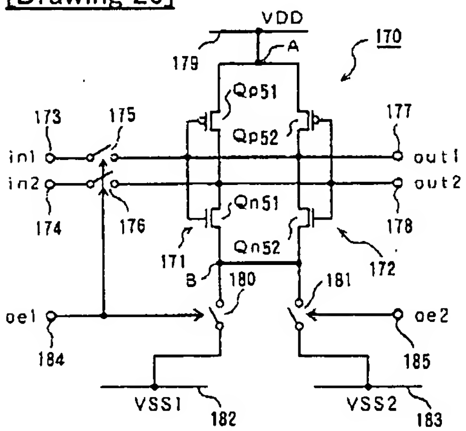
[Drawing 24]



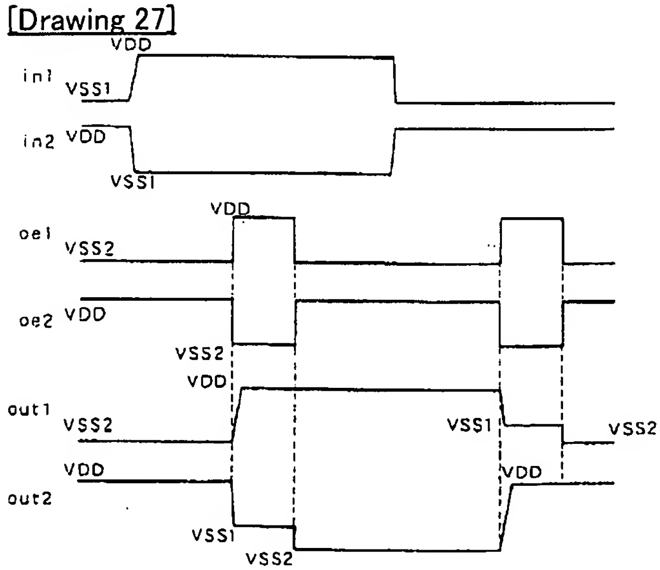
[Drawing 25]



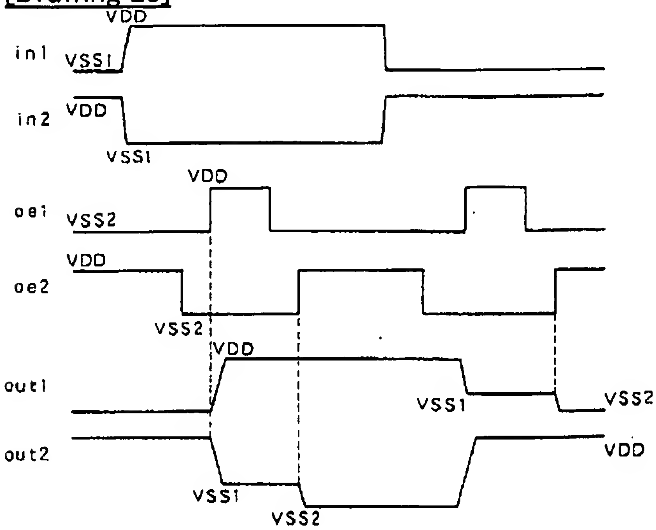
[Drawing 26]



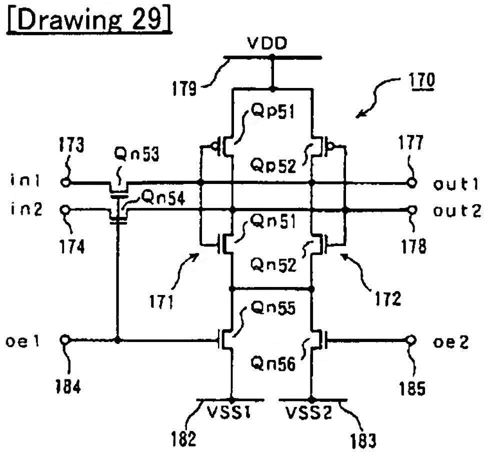
[Drawing 27]



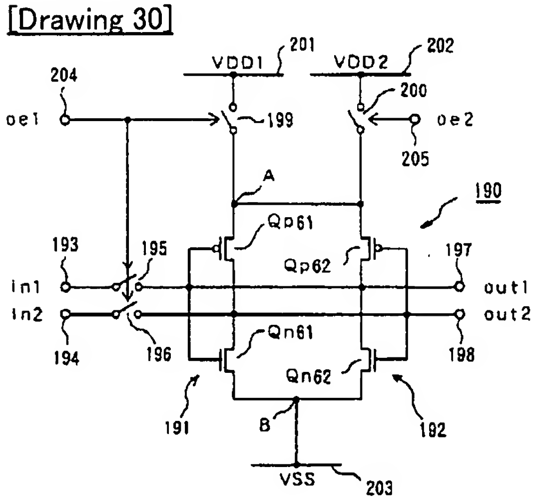
[Drawing 28]



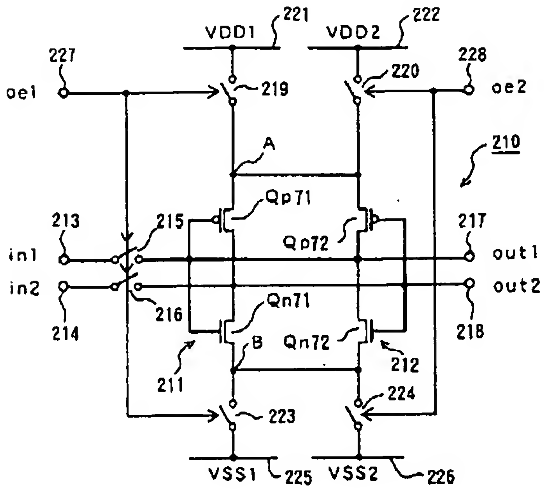
[Drawing 29]



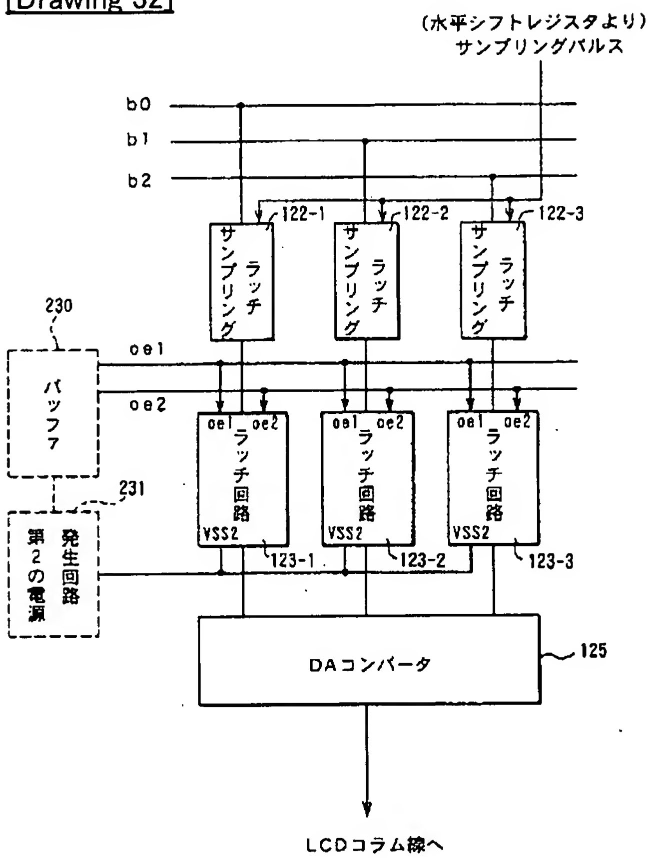
[Drawing 30]



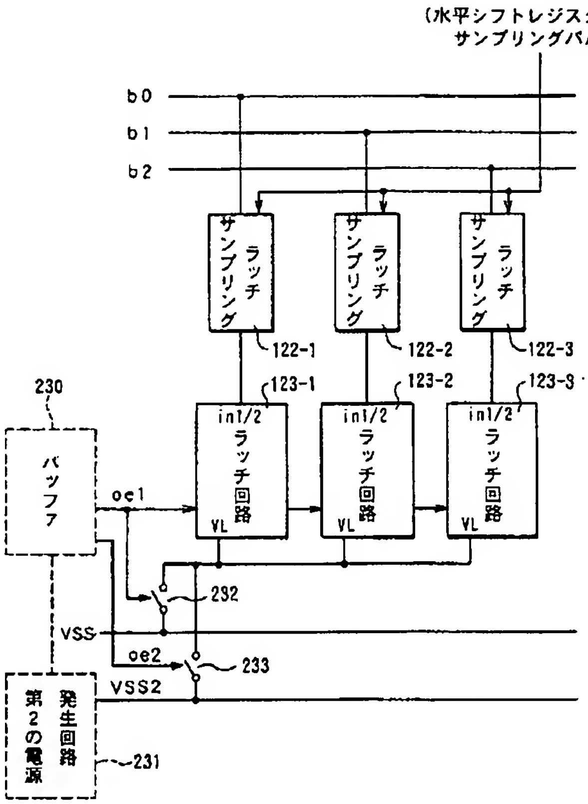
[Drawing 31]



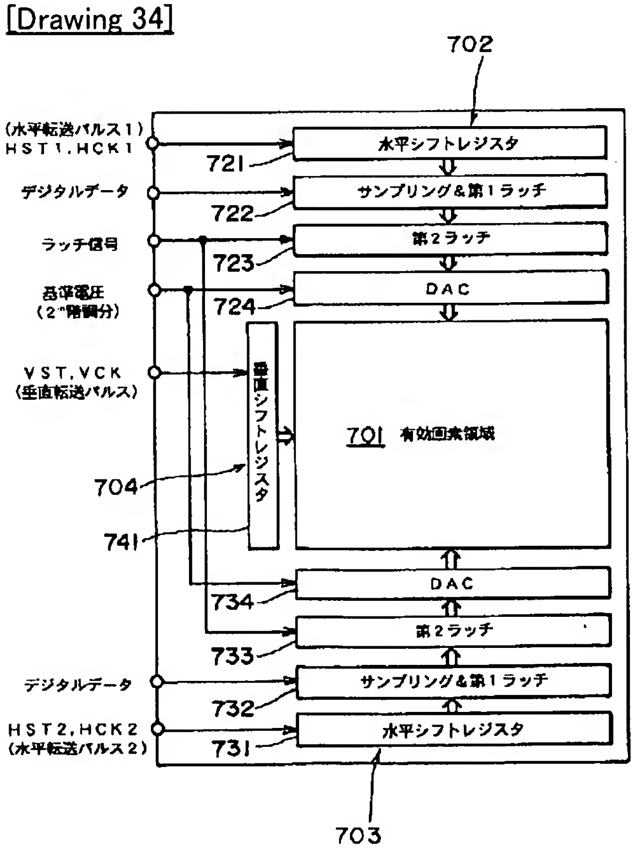
[Drawing 32]



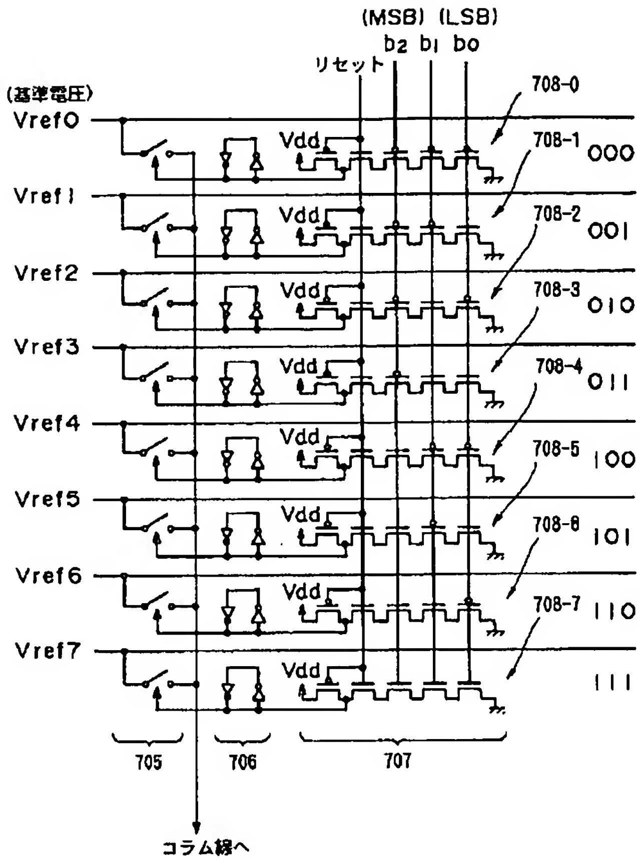
[Drawing 33]



[Drawing 34]



[Drawing 35]



[Translation done.]